dscal
DIGITAL SYSTEMS & COMPUTER ARCHITECTURE LABORATORY

Εργαστήριο Σχεδίασης Ψηφιακών Συστημάτων

3ο Εργαστηριακό Μάθημα

Βασιλόπουλος Διονύσης

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ΤΜΗΜΑ ΠΛΗΡΟΦΟΡΙΚΗΣ & ΤΗΛΕΠΙΚΟΙΝΩΝΙΩΝ

3η Εργαστηριακή Άσκηση

Ανάλυση άσκησης

Δημιουργία νέου Ρολογιού
=
100 εκ. χτύποι του CLK της κάρτας

Υπολογισμός επόμενης κατάστασης

Ενημέρωση Τρέχουσας Κατάστασης

Υπολογισμός εξόδου

4η Εργαστηριακή Άσκηση

ΠΡΟΧΩΡΗΣΤΕ ΣΤΗΝ ΑΣΚΗΣΗ

4η Εργαστηριακή Άσκηση

Αρχιτεκτονική (1/4) – Νέο Ρολόι (Περίοδος = 1 sec)

```
signal clk_100MHz: std_logic;
signal sum: unsigned(6 downto 0);
signal bcd_rd: unsigned(3 downto 0);
signal bcd_ld: unsigned(3 downto 0);
signal seven_segment_left: std_logic_vector(6 downto 0);
signal seven_segment_right: std_logic_vector(6 downto 0);
signal digit_selection: std_logic;
```

```
One_sec_clk : process (clk, reset) is
variable clk_ticks : integer;

begin
        if reset = '1' then
          clk_100MHz<='0';
          clk_ticks :=0;
        elsif rising_edge(clk) then
                if clk_ticks = 99999999 then
                        clk_ticks := 0;
                        clk_100MHz<= '1';
                else
                        clk_ticks := clk_ticks + 1;
                        clk_100MHz <= '0';
                end if; -- clk_ticks
        end if; --reset
end process One_sec_clk;
```

4η Εργαστηριακή Άσκηση

Αρχιτεκτονική (2/4) – Tick Counter per second

Αρχιτεκτονική →

```
count: process (clk_100MHz, reset) is
begin
if (reset='1') then
   counts<=(others=>'0');
elsif rising_edge(clk_100MHz) then
   if direction='1' then
      if sum<99 then
         sum<=sum+1;
      else
         sum<=(others=>'0');
      end if; -- sum<99
   else
      if sum>0 then
         sum<=sum-1;
      else
         sum<="1100011";
      end if; -- sum>0
   end if; --direction
end if; --reset
end process count;
```

4η Εργαστηριακή Άσκηση

Αρχιτεκτονική (3/4) – Switch every 0.05 sec to each digit

Αρχιτεκτονική →

```
digit_process: process (clk, reset) is
variable clk_ticks : integer;
begin
if reset = '1' then
      clk_ticks :=0;
      digit_selection<='0';
      seven_segment<=(others=>'0');
elsif rising_edge(clk) then
      if clk_ticks = 500000 then
         clk_ticks := 0;
         if digit_selection='0' then
                  digit_selection<='1’;
                  seven_segment<=seven_segment_left;
         else
                  digit_selection<='0';
                  seven_segment<=seven_segment_right;
         end if;
         else
                  clk_ticks := clk_ticks + 1;
         end if; -- clk_ticks
end if; --reset
end process digit_process;
```

4η Εργαστηριακή Άσκηση

Αρχιτεκτονική (4/4) – Output signals

```
led_result<=std_logic_vector(counts);
bcd_ld<=resize(sum/10, bcd_ld'length);              --Tens
bcd_rd<=resize(sum mod 10, bcd_rd'length);          --Units

bcd_right_digit_values: process (bcd_rd) begin
case bcd_rd is
   when X"0" => seven_segment   <="0111111";   -- 0
   when X"1" => seven_segment   <="0000110";   -- 1
   when X"2" => seven_segment   <="1011011";   -- 2
   when X"3" => seven_segment   <="1001111";   -- 3
   when X"4" => seven_segment   <="1100110";   -- 4
   when X"5" => seven_segment   <="1101101";   -- 5
   when X"6" => seven_segment   <="1111101";   -- 6
   when X"7" => seven_segment   <="0000111";   -- 7
   when X"8" => seven_segment   <="1111111";   -- 8
   when X"9" => seven_segment   <="1101111";   -- 9
   when others => seven_segment <="0000000";
end case;
end process bcd_right_digit_values;
```

```
bcd_left_digit_values: process (bcd_ld) begin
case bcd_ld is
   when X"0" => seven_segment_left   <="0111111";   -- 0
   when X"1" => seven_segment_left   <="0000110";   -- 1
   when X"2" => seven_segment_left   <="1011011";   -- 2
   when X"3" => seven_segment_left   <="1001111";   -- 3
   when X"4" => seven_segment_left   <="1100110";   -- 4
   when X"5" => seven_segment_left   <="1101101";   -- 5
   when X"6" => seven_segment_left   <="1111101";   -- 6
   when X"7" => seven_segment_left   <="0000111";   -- 7
   when X"8" => seven_segment_left   <="1111111";   -- 8
   when X"9" => seven_segment_left   <="1101111";   -- 9
   when others => seven_segment_left <="0000000";
end case;
end process bcd_left_digit_values;

digit_selection_out<=digit_selection;
```

4η Εργαστηριακή Άσκηση

Constraints (1/2) – CLK + Switches + Leds

Constraints →

```
# CLK - Zedboard 100MHz oscillator
set_property -dict { PACKAGE_PIN Y9 IOSTANDARD LVCMOS33 } [get_ports {clk}]

##############################
# On-board Slide Switches  #
##############################
set_property -dict { PACKAGE_PIN M15   IOSTANDARD LVCMOS33 } [get_ports { reset }];
set_property -dict { PACKAGE_PIN F22   IOSTANDARD LVCMOS33 } [get_ports { direction }];

##############################
# On-board LEDS  #
##############################
set_property -dict { PACKAGE_PIN T22   IOSTANDARD LVCMOS33 } [get_ports { led_result[0] }];
set_property -dict { PACKAGE_PIN T21   IOSTANDARD LVCMOS33 } [get_ports { led_result[1] }];
set_property -dict { PACKAGE_PIN U22   IOSTANDARD LVCMOS33 } [get_ports { led_result[2] }];
set_property -dict { PACKAGE_PIN U21   IOSTANDARD LVCMOS33 } [get_ports { led_result[3] }];
set_property -dict { PACKAGE_PIN V22   IOSTANDARD LVCMOS33 } [get_ports { led_result[4] }];
set_property -dict { PACKAGE_PIN W22   IOSTANDARD LVCMOS33 } [get_ports { led_result[5] }];
set_property -dict { PACKAGE_PIN U19   IOSTANDARD LVCMOS33 } [get_ports { led_result[6] }];
```

4η Εργαστηριακή Άσκηση

Constraints (1/2) – Pmod + CLK

Constraints →

```
##############################
# PmodSSO                    #
##############################

set_property -dict { PACKAGE_PIN Y11   IOSTANDARD LVCMOS33 } [get_ports { seven_segment[0] }];
set_property -dict { PACKAGE_PIN AA11  IOSTANDARD LVCMOS33 } [get_ports { seven_segment[1] }];
set_property -dict { PACKAGE_PIN Y10   IOSTANDARD LVCMOS33 } [get_ports { seven_segment[2] }];
set_property -dict { PACKAGE_PIN AA9   IOSTANDARD LVCMOS33 } [get_ports { seven_segment[3] }];
set_property -dict { PACKAGE_PIN W12   IOSTANDARD LVCMOS33 } [get_ports { seven_segment[4] }];
set_property -dict { PACKAGE_PIN W11   IOSTANDARD LVCMOS33 } [get_ports { seven_segment[5] }];
set_property -dict { PACKAGE_PIN V10   IOSTANDARD LVCMOS33 } [get_ports { seven_segment[6] }];

set_property -dict { PACKAGE_PIN W8   IOSTANDARD LVCMOS33 } [get_ports { digit_selection_out }];

##############################################################
##ZedBoard Timing Constraints
##############################################################
# define clock and period
create_clock -period 10 -name CLK -waveform {0.000 5.000} [get_ports {clk}]
```

4η Εργαστηριακή Άσκηση

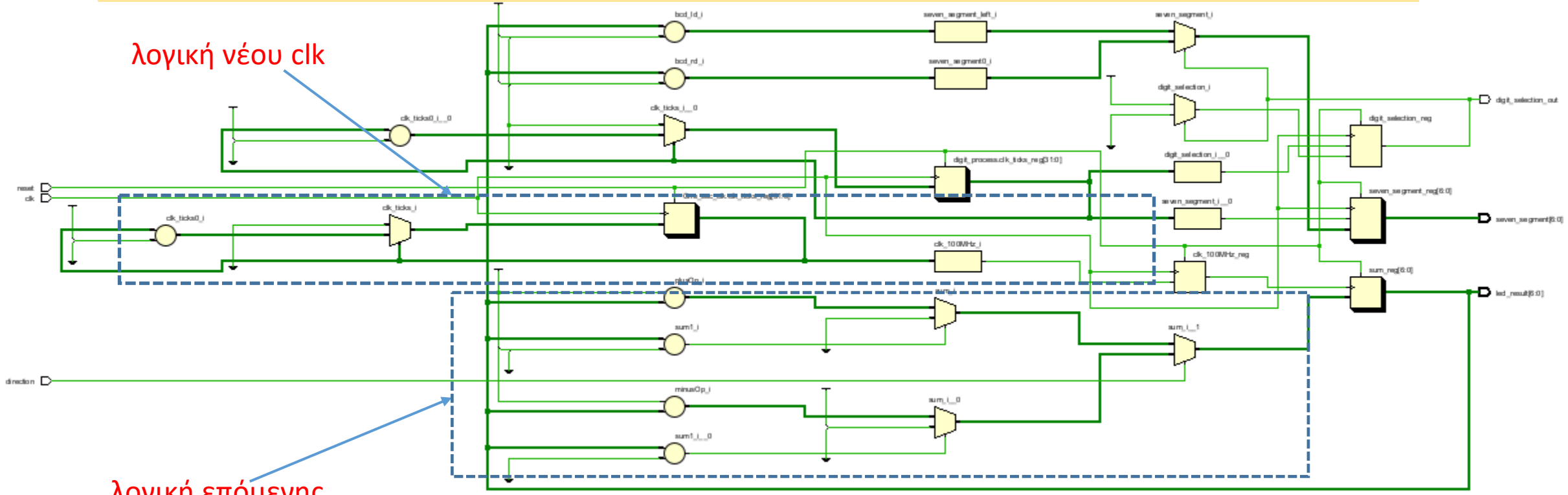
Pmod Manual

Manual Pmod

https://reference.digilentinc.com/reference/pmod/pmodssd/reference-manual

4η Εργαστηριακή Άσκηση

RTL Design

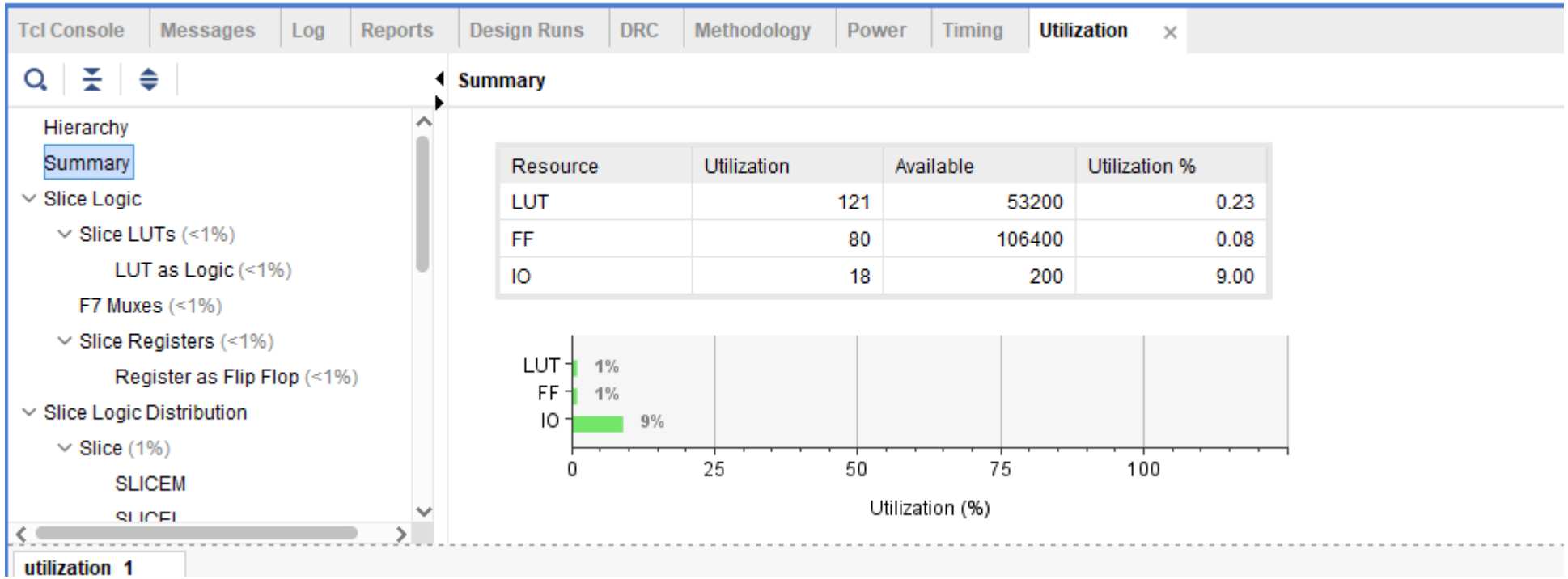


4η Εργαστηριακή Άσκηση

Synthesis/Implementation – Schematic

4η Εργαστηριακή Άσκηση

Implementation – Report Utilization

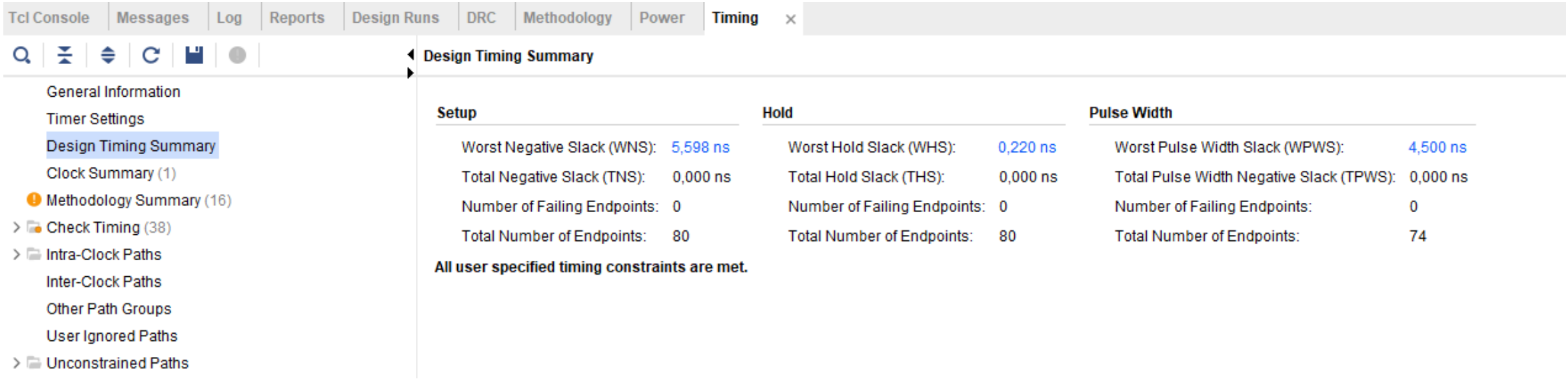


Και από Project Summary

4η Εργαστηριακή Άσκηση

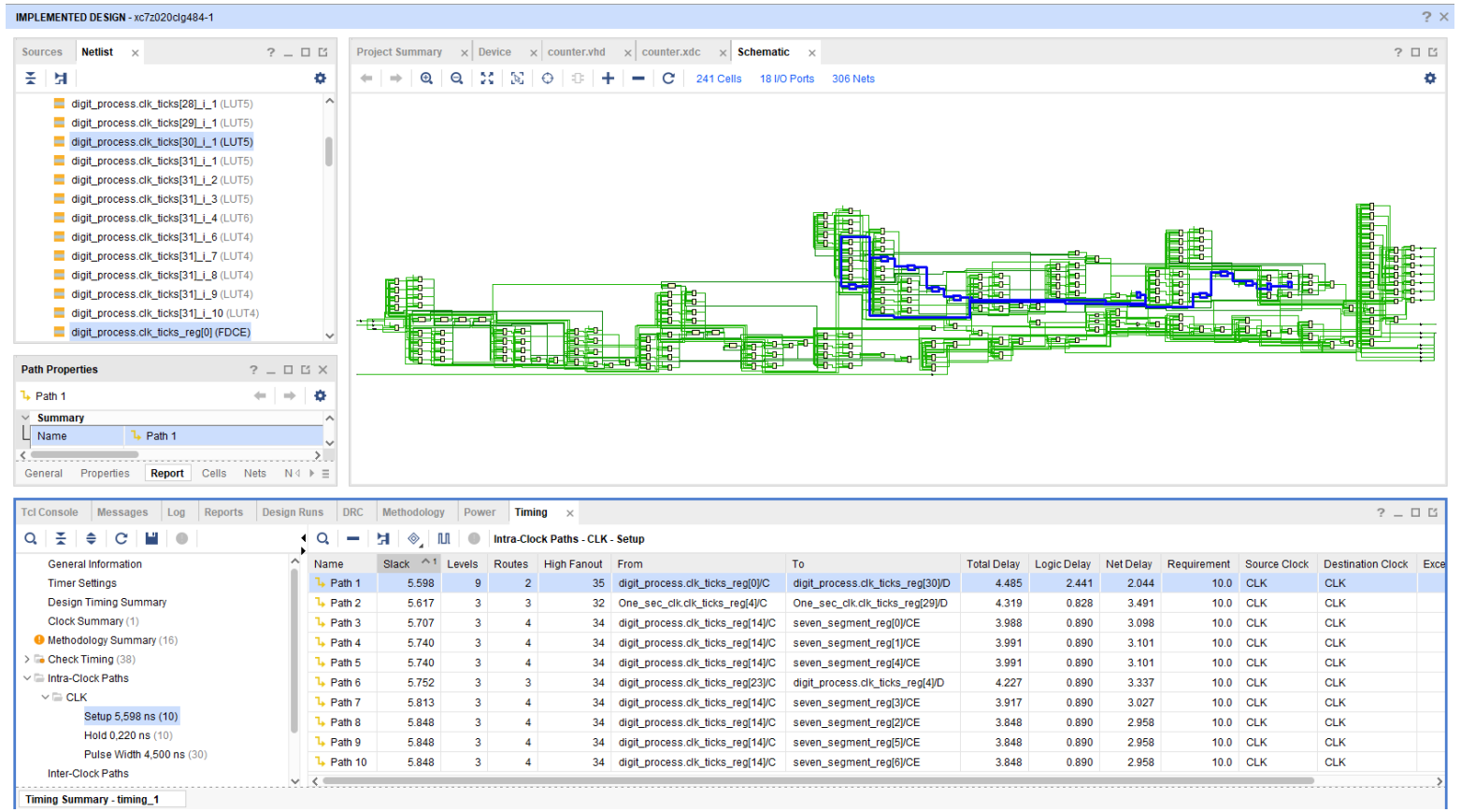
Implementation – Timing Reports (1/4)

Menu Reports->Timing-> Report Timing Summary
ή
Open Implemented Design->Report Timing Summary



4η Εργαστηριακή Άσκηση

Implementation – Timing Reports (2/4) - Setup

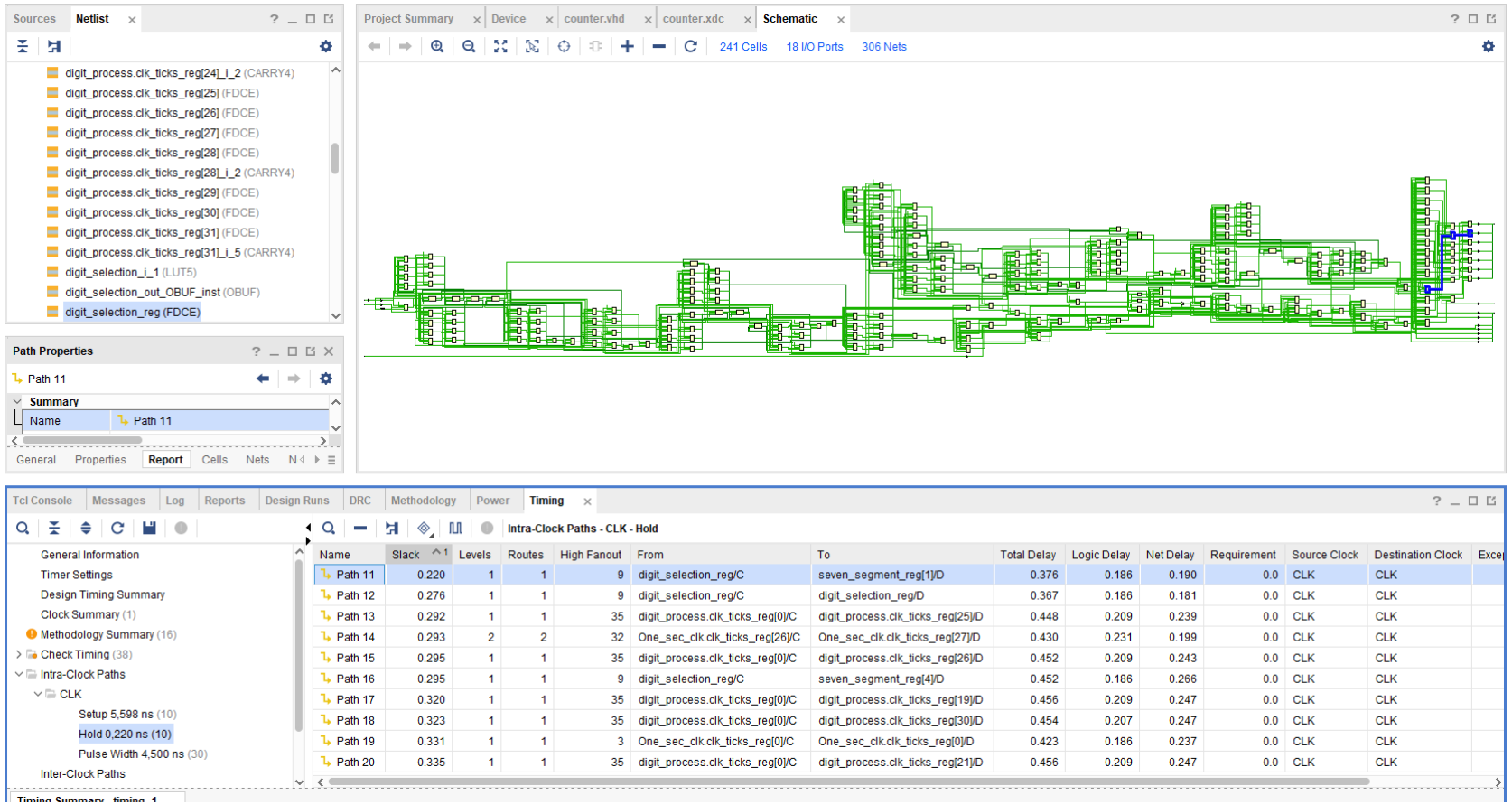


Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock
Path 1	5.598	9	2	35	digit_process.clk_ticks_reg[0]/C	digit_process.clk_ticks_reg[30]/D	4.485	2.441	2.044	10.0	CLK	CLK
Path 2	5.617	3	3	32	One_sec_clk.clk_ticks_reg[4]/C	One_sec_clk.clk_ticks_reg[29]/D	4.319	0.828	3.491	10.0	CLK	CLK
Path 3	5.707	3	4	34	digit_process.clk_ticks_reg[14]/C	seven_segment_reg[0]/CE	3.988	0.890	3.098	10.0	CLK	CLK
Path 4	5.740	3	4	34	digit_process.clk_ticks_reg[14]/C	seven_segment_reg[1]/CE	3.991	0.890	3.101	10.0	CLK	CLK
Path 5	5.740	3	4	34	digit_process.clk_ticks_reg[14]/C	seven_segment_reg[4]/CE	3.991	0.890	3.101	10.0	CLK	CLK
Path 6	5.752	3	3	34	digit_process.clk_ticks_reg[23]/C	digit_process.clk_ticks_reg[4]/D	4.227	0.890	3.337	10.0	CLK	CLK
Path 7	5.813	3	4	34	digit_process.clk_ticks_reg[14]/C	seven_segment_reg[3]/CE	3.917	0.890	3.027	10.0	CLK	CLK
Path 8	5.848	3	4	34	digit_process.clk_ticks_reg[14]/C	seven_segment_reg[2]/CE	3.848	0.890	2.958	10.0	CLK	CLK
Path 9	5.848	3	4	34	digit_process.clk_ticks_reg[14]/C	seven_segment_reg[5]/CE	3.848	0.890	2.958	10.0	CLK	CLK
Path 10	5.848	3	4	34	digit_process.clk_ticks_reg[14]/C	seven_segment_reg[6]/CE	3.848	0.890	2.958	10.0	CLK	CLK

Setup Time:
Αναφέρεται στις αργές διαδρομές (καθυστέρηση διάδοσης)

4η Εργαστηριακή Άσκηση

Implementation – Timing Reports (3/4) - Hold



Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock
Path 11	0.220	1	1	9	digit_selection_reg/C	seven_segment_reg[1]/D	0.376	0.186	0.190	0.0	CLK	CLK
Path 12	0.276	1	1	9	digit_selection_reg/C	digit_selection_reg/D	0.367	0.186	0.181	0.0	CLK	CLK
Path 13	0.292	1	1	35	digit_process.clk_ticks_reg[0]/C	digit_process.clk_ticks_reg[25]/D	0.448	0.209	0.239	0.0	CLK	CLK
Path 14	0.293	2	2	32	One_sec_clk.clk_ticks_reg[26]/C	One_sec_clk.clk_ticks_reg[27]/D	0.430	0.231	0.199	0.0	CLK	CLK
Path 15	0.295	1	1	35	digit_process.clk_ticks_reg[0]/C	digit_process.clk_ticks_reg[26]/D	0.452	0.209	0.243	0.0	CLK	CLK
Path 16	0.295	1	1	9	digit_selection_reg/C	seven_segment_reg[4]/D	0.452	0.186	0.266	0.0	CLK	CLK
Path 17	0.320	1	1	35	digit_process.clk_ticks_reg[0]/C	digit_process.clk_ticks_reg[19]/D	0.456	0.209	0.247	0.0	CLK	CLK
Path 18	0.323	1	1	35	digit_process.clk_ticks_reg[0]/C	digit_process.clk_ticks_reg[30]/D	0.454	0.207	0.247	0.0	CLK	CLK
Path 19	0.331	1	1	3	One_sec_clk.clk_ticks_reg[0]/C	One_sec_clk.clk_ticks_reg[0]/D	0.423	0.186	0.237	0.0	CLK	CLK
Path 20	0.335	1	1	35	digit_process.clk_ticks_reg[0]/C	digit_process.clk_ticks_reg[21]/D	0.456	0.209	0.247	0.0	CLK	CLK

Hold Time:
Αναφέρεται στις γρήγορες διαδρομές (καθυστέρηση μόλυνσης)

4η Εργαστηριακή Άσκηση

Implementation – Timing Reports (4/4)

TCL Console>*report_timing_summary –datasheet*

(FULL REPORT)

Εμφανίζεται στη TCL console