Υλοποίηση Ολοκληρωμένων Ψηφιακών Κυκλωμάτων

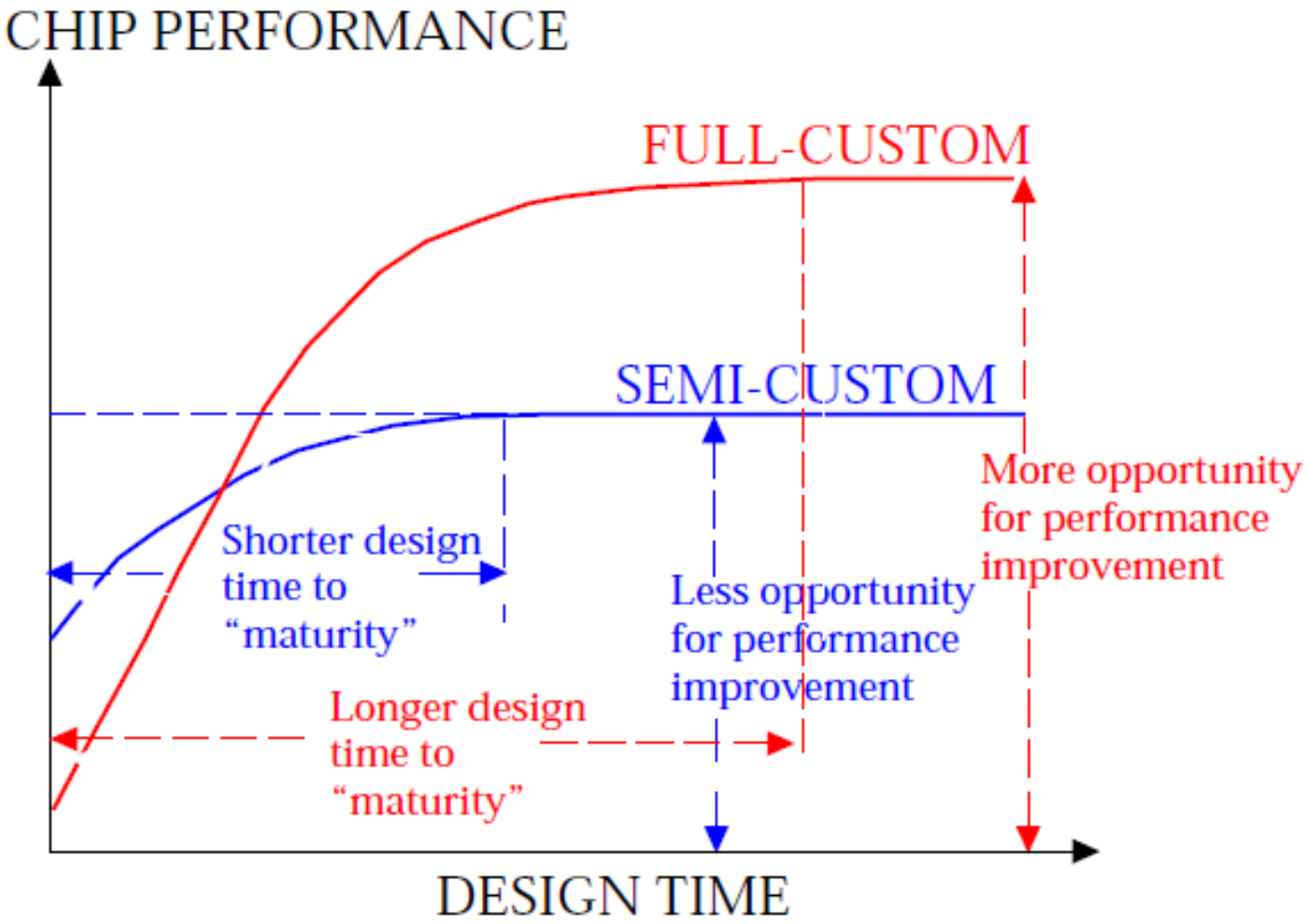
ΒΙΒΛΙΟΓΡΑΦΙΑ

1. “Principles of CMOS LLSI Design”, N. Weste, K. Eshraghian, Addison Wesley.
2. “CMOS VLSI Design”, N. Weste, D. Harris, Addison Wesley.
3. “CMOS Digital Integrated Circuits”, S-M. Kang, Y. Leblebici, McGRAW-HILL.
4. “Digital Integrated Circuits”, J. Rabaey, A. Chandrakasan, B. Nokolic, PEARSON.

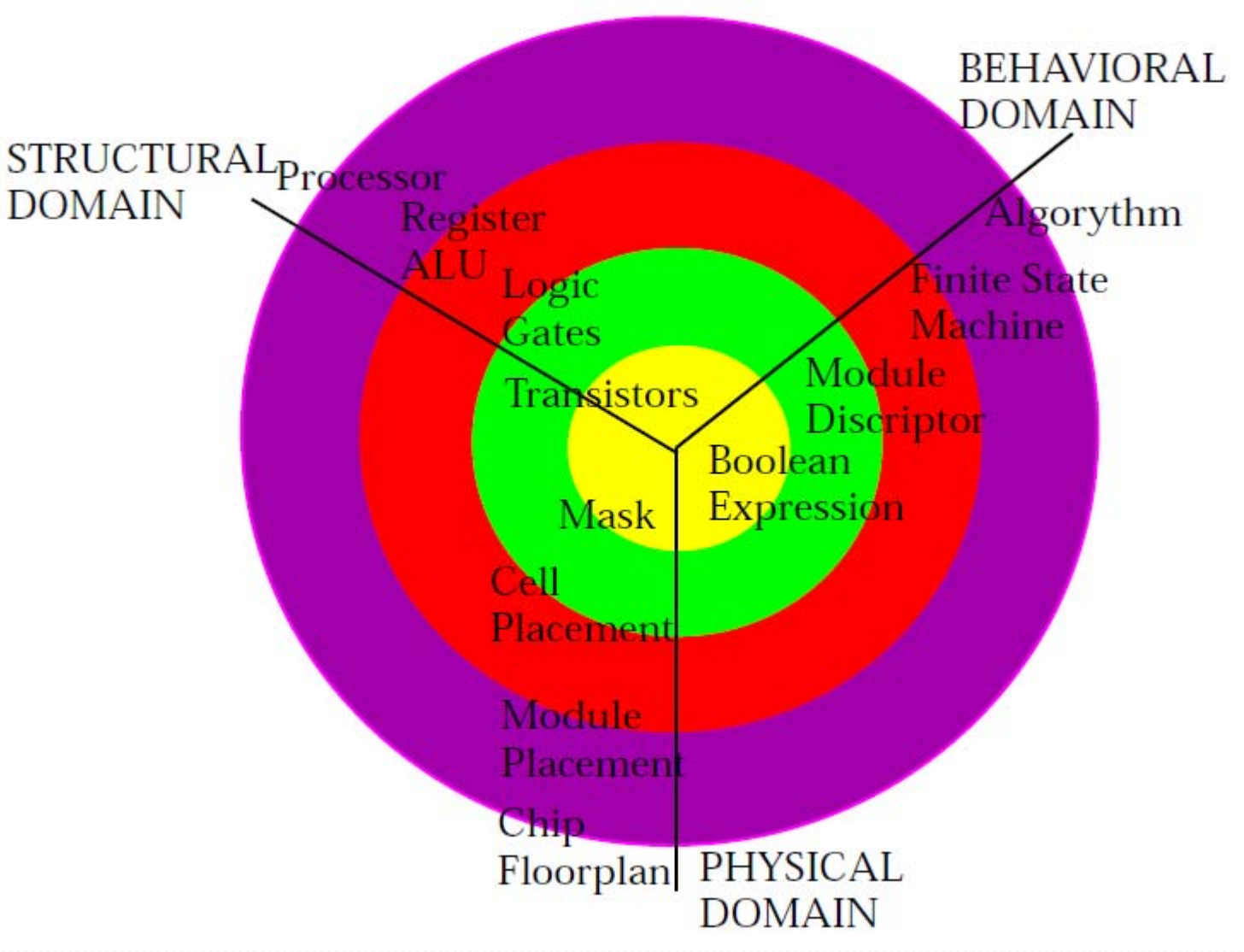
ΣΤΟΧΟΙ ΤΗΣ ΜΟΝΟΛΙΘΙΚΗΣ ΟΛΟΚΛΗΡΩΣΗΣ

-> LESS AREA, MORE COMPACTNESS AT ALL SYSTEM LEVELS
-> LESS POWER CONSUMPTION
-> LESS TESTING (MORE COMPLEX TESTING)
-> HIGHER RELIABILITY, DUE TO IMPROVED ON-CHIP INTERCONNECTS
-> HIGHER SPEED DUE TO REDUCED INTERCONNECT LENGTH
-> SIGNIFICANT COST SAVINGS

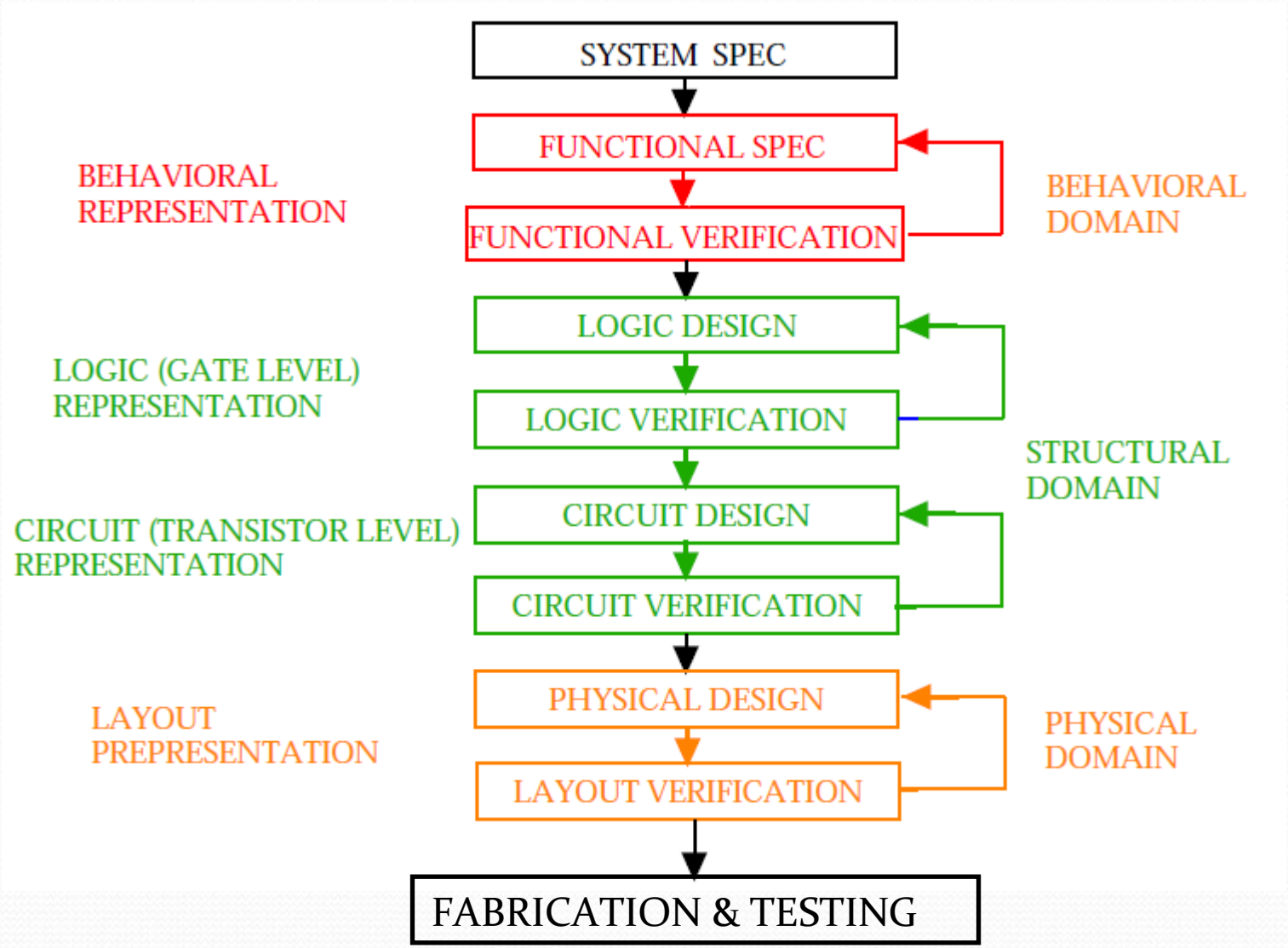
ΕΠΙΔΡΑΣΗ ΤΗΣ ΜΕΘΟΔΟΛΟΓΙΑΣ ΣΧΕΔΙΑΣΗΣ



ΣΧΕΔΙΑΣΤΙΚΑ ΕΠΙΠΕΔΑ ΑΦΑΙΡΕΣΗΣ



ΡΟΗ ΣΧΕΔΙΑΣΗΣ VLSI ΚΥΚΛΩΜΑΤΩΝ



ΣΤΡΑΤΗΓΙΚΕΣ ΔΟΜΗΜΕΝΗΣ ΣΧΕΔΙΑΣΗΣ

Techniques evolved for complex harware and software projects.

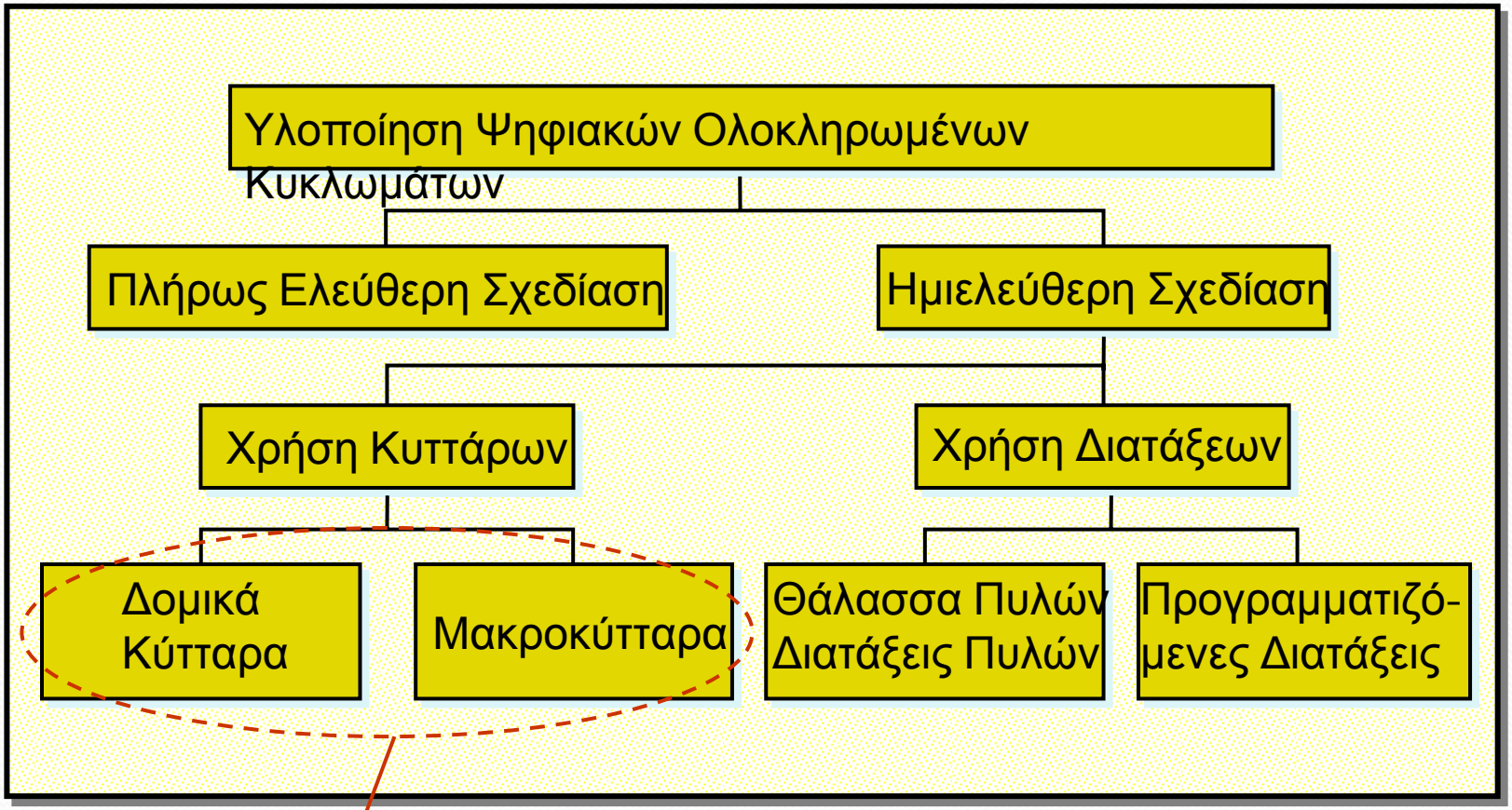
-> Hierarchy: Subdivide the design into many levels of sub-modules

-> Regularity: Subdivide to max number of similar sub-modules at each level

-> Modularity: Define sub-modules unambiguously & well defined interfaces

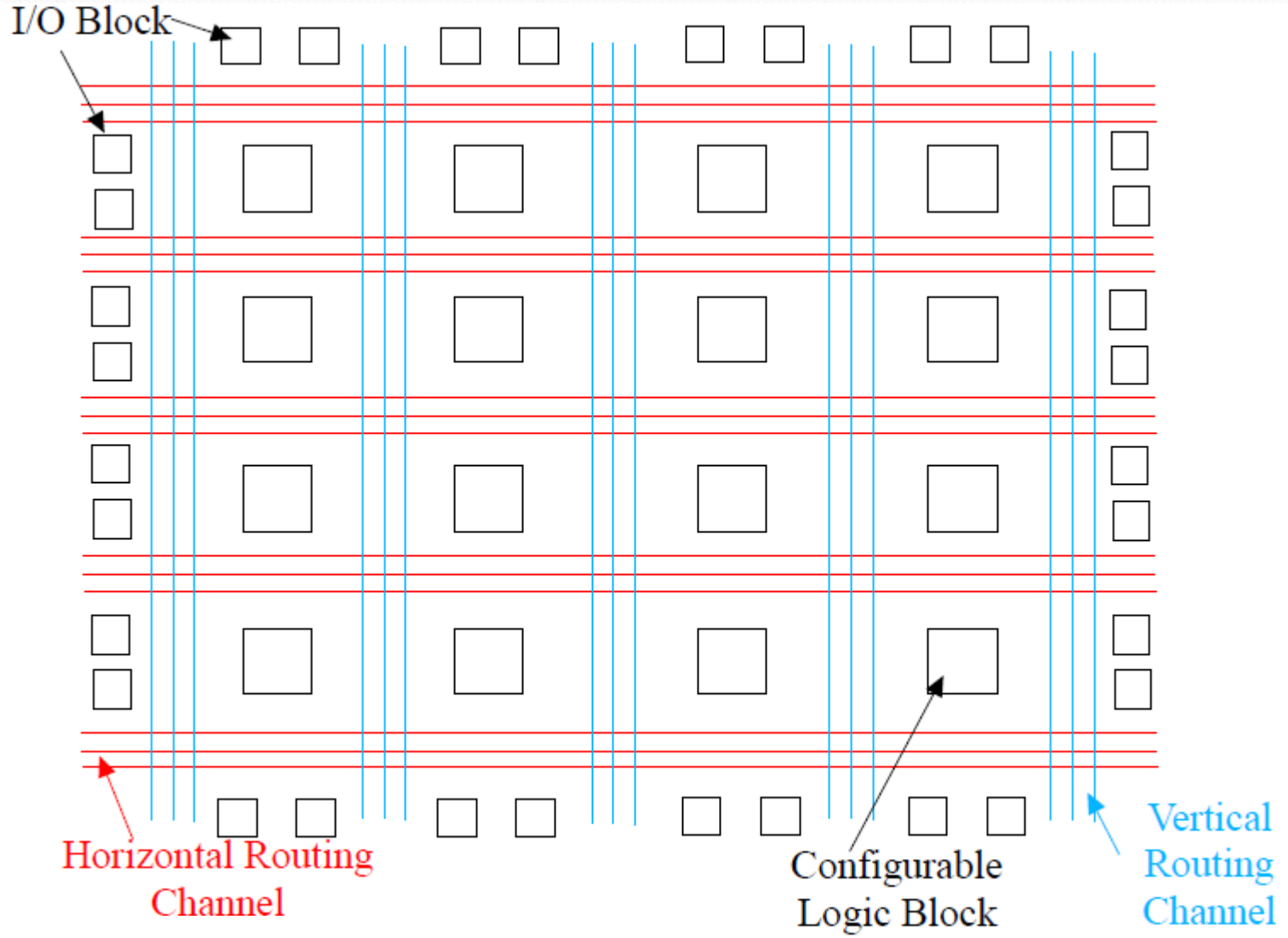
-> Locality: Max local connections, keeping critical paths within module boundaries

ΣΧΕΔΙΑΣΤΙΚΕΣ ΕΠΙΛΟΓΕΣ

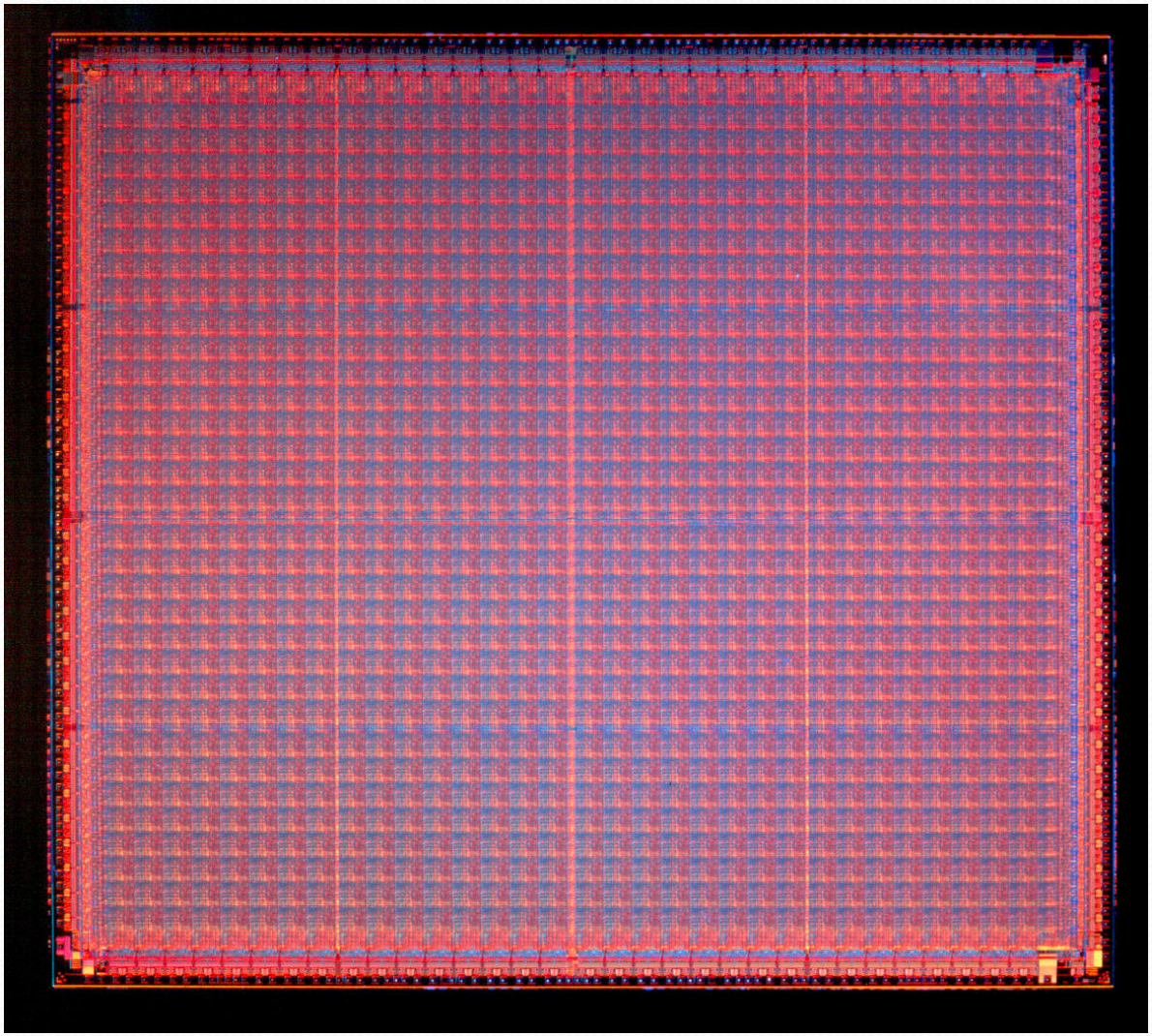


Σχεδίαση Ολοκληρωμένων Κυκλωμάτων Ειδικών Εφαρμογών
Application Specific Integrated Circuits (ASICs)

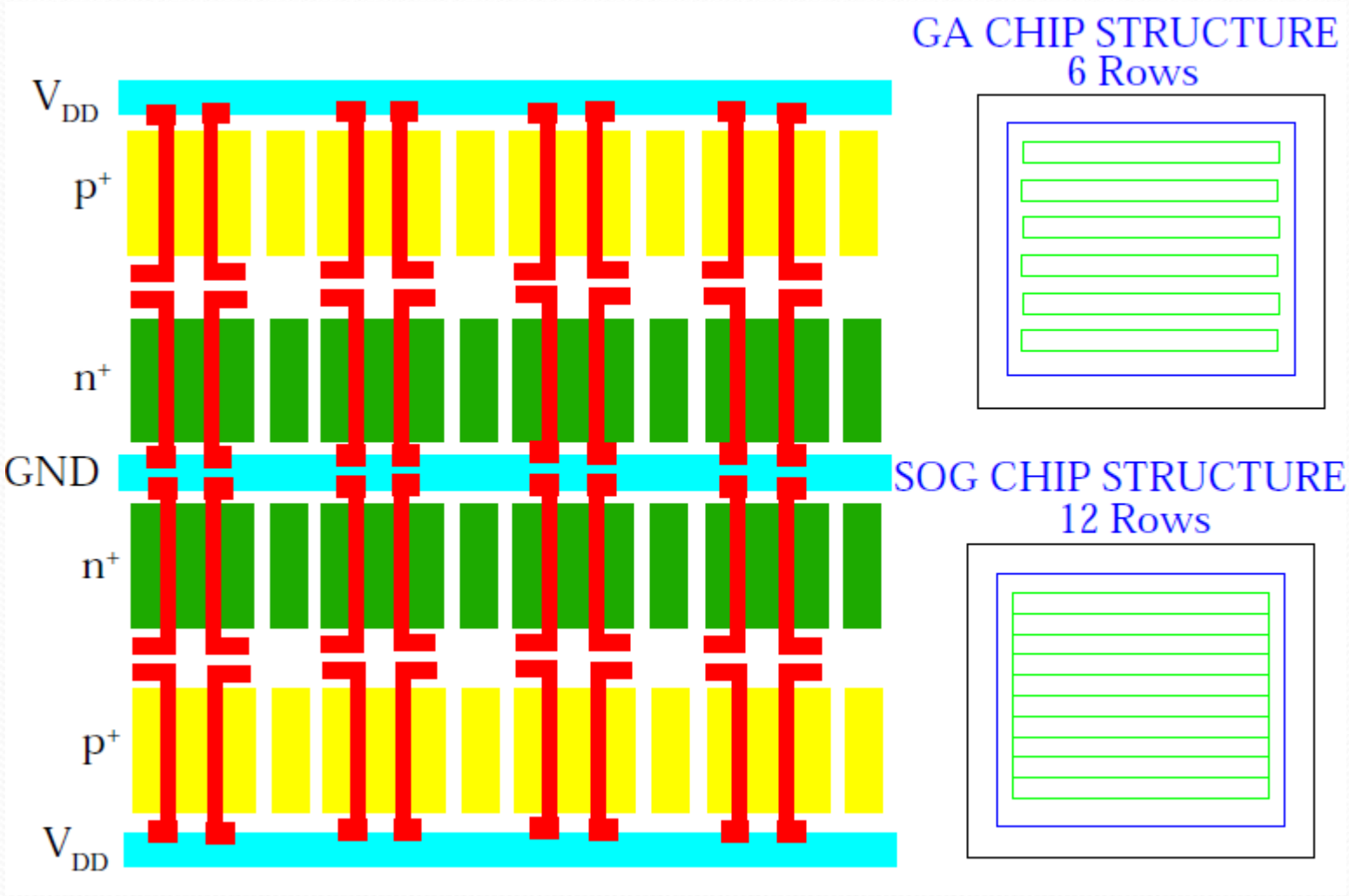
FIELD PROGRAMMABLE GATE ARRAY (FPGA)



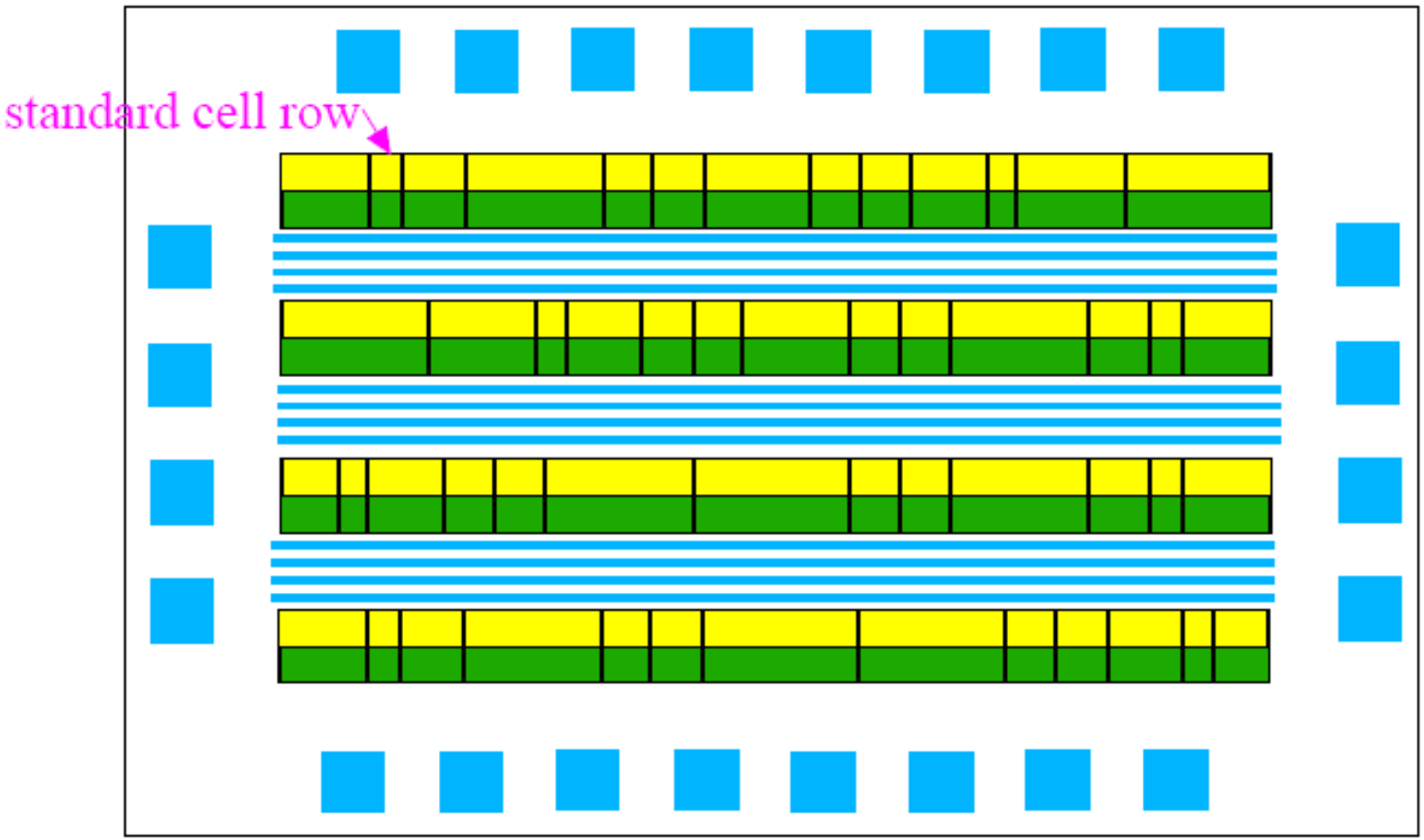
ΟΛΟΚΛΗΡΩΜΕΝΟ FPGA



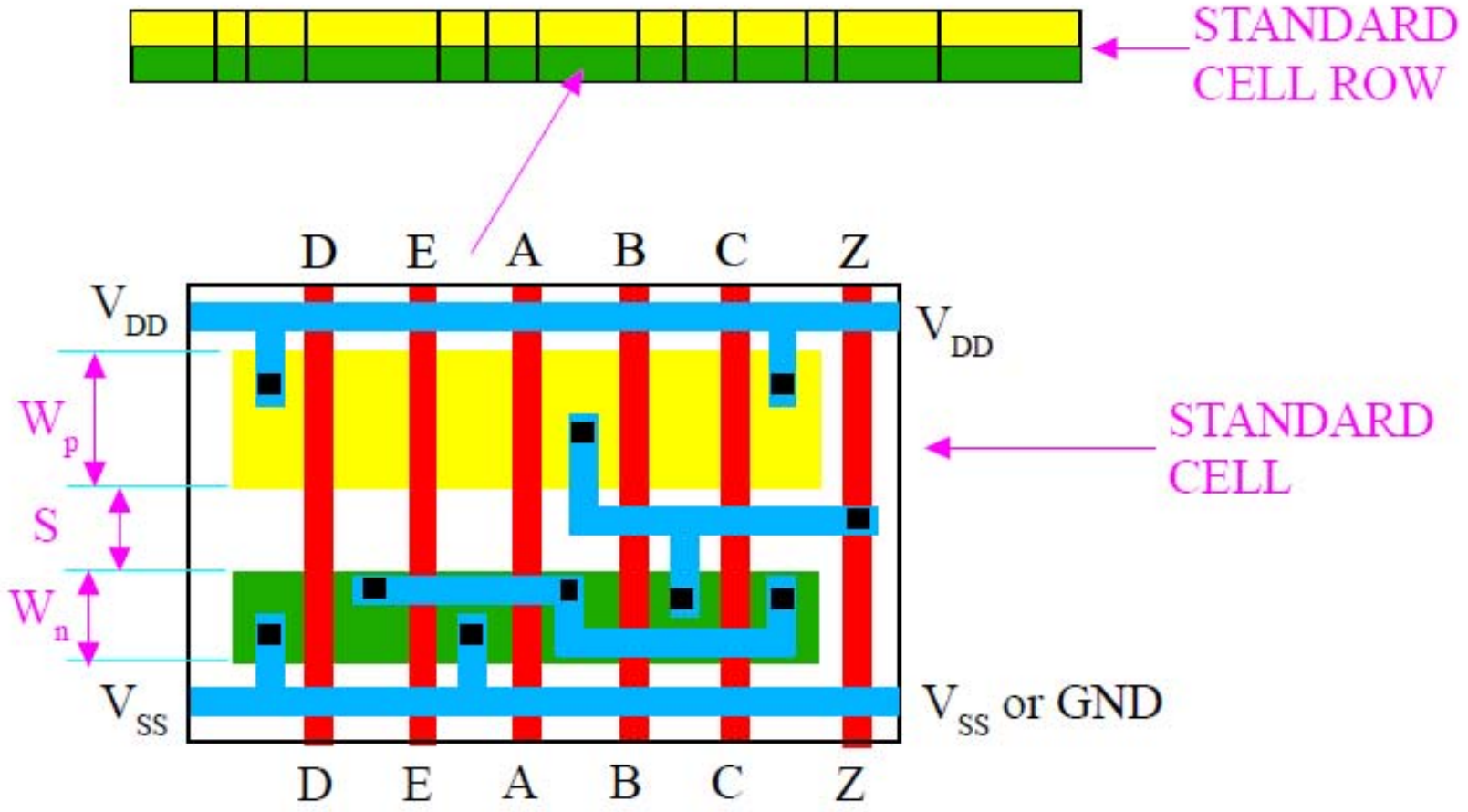
SEA OF GATES / GATE ARRAY



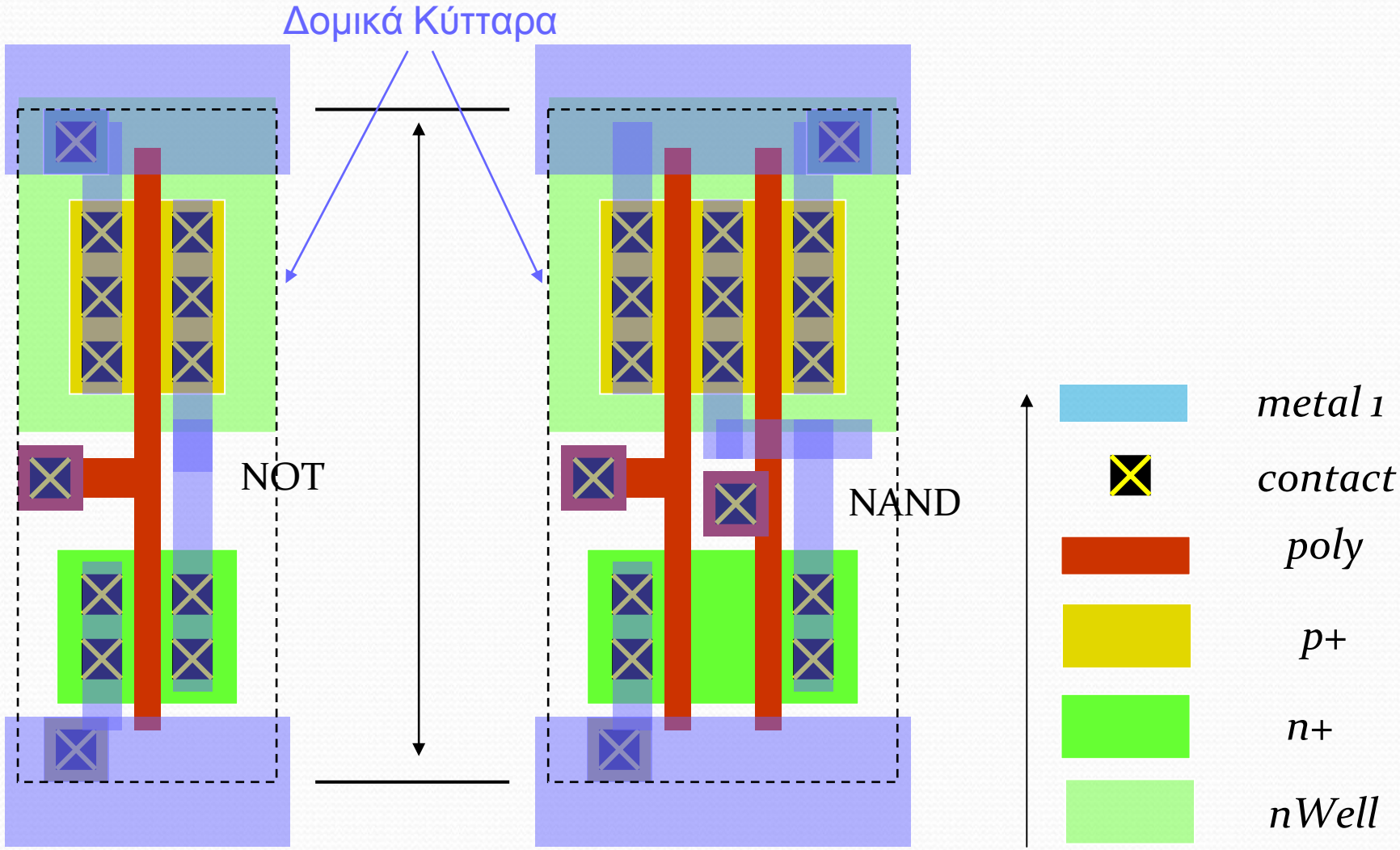
ΣΧΕΔΙΑΣΗ ΜΕ ΔΟΜΙΚΑ ΚΥΤΤΑΡΑ (STANDARD CELLS)



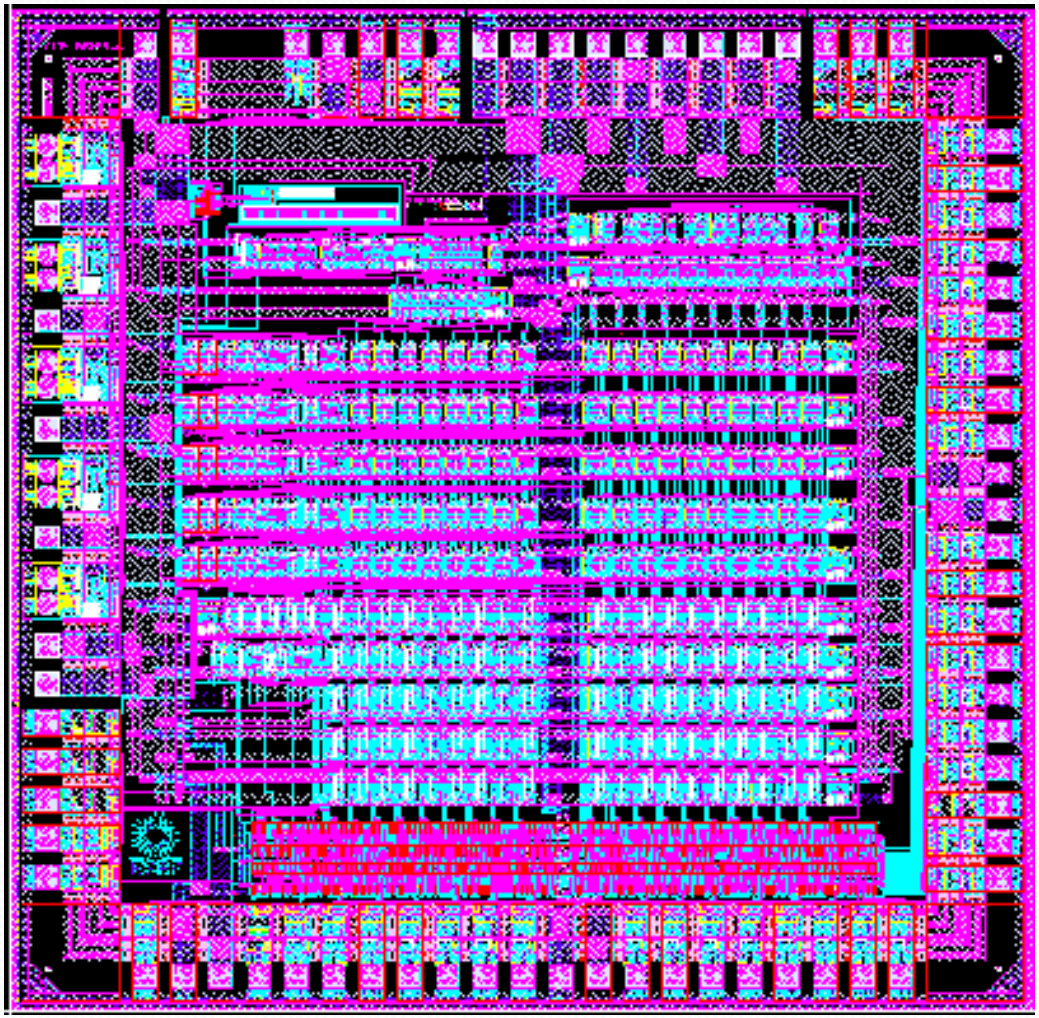
ΔΟΜΙΚΑ ΚΥΤΤΑΡΑ (STANDARD CELLS)



ΠΛΗΡΩΣ ΕΛΕΥΘΕΡΗ ΣΧΕΔΙΑΣΗ (FULL CUSTOM)



ΠΛΗΡΗΣ ΕΙΚΟΝΑ ΟΛΟΚΛΗΡΩΜΕΝΟΥ



ΠΟΙΟΤΗΤΑ ΣΧΕΔΙΑΣΗΣ

-> ACHIEVE SPECIFICATIONS (Static & Dynamic)

->DIE SIZE

->POWER DISSIPATION

-> TESTABILITY

-> YIELD AND MANUFACTURABILITY

-> RELIABILITY

->TECHNOLOGY UPDATABLE

-> TESTABILITY

+ generation of good test vectors
+ availablity of reliable test fixture at speed
+ design of testable chip

-> YIELD AND MANUFACTURABILITY

+ functional yield
+ parametric yield

->RELIABILITY

+ premature aging (Infant mortality)
+ ESD/EOS
+ latchup
+ on-chip noise and crosstalk
+ power and ground bouncing

->TECHNOLOGY UPDATABLE

+ Easily updated to new design rules

ΠΑΚΕΤΑΡΙΣΜΑ (PACKAGING)

DUAL IN-LINE PACKAGE (DIP)

1. ceramic or plastic pin-through-hole (PTH)
2. low cost, but large size
3. high lead inductance (22 - 36 nH)
4. max pin count usually 64

PIN GRID ARRAY (PGA) PACKAGE

1. ceramic or plastic pin-through-hole (PTH)
2. higher pin count (100 - 400 pins)
3. higher cost than DIP

CHIP CARRIER PACKAGE (CCP)

1. surface-mounted technology (SMT)
2. leadless chip carrier supports high pin count
3. more efficient use of PCB area than DIP or PGA

MULTI-CHIP MODULE (MCM)

1. multiple chips assembled on a common substrate
2. high performance applications
3. most efficient use of PCB area

ΕΡΓΑΛΕΙΑ ΣΧΕΔΙΑΣΗΣ (VLSI CAD TOOLS)

CATAGORIES OF CAD TOOLS

1. High Level Synthesis (HDLs)
2. Logic Synthesis
3. Circuit Optimization
   a. transistor sizing for min delays
   b. process variations
   c. statistical design
4. Layout
   a. floorplanning
   b. place & route
   c. module generation
   d. automatic cell placement and routing
5. Layout Extraction
6. Simulation (SPICE for circuit-level simulation)
7. Layout - Schematic Verification
8. Design Rule Check