



dscal
DIGITAL SYSTEMS & COMPUTER ARCHITECTURE LABORATORY

Εργαστήριο Λογικής Σχεδίασης

4^ο Εργαστηριακό Μάθημα

Βασιλόπουλος Διονύσης

Ε.Δι.Π. Τμήματος Πληροφορικής & Τηλεπικοινωνιών - ΕΚΠΑ

4^η Εργαστηριακή Άσκηση

Ανάλυση άσκησης

A

Μετρώ 10000000 χτύπους
=
1 sec

Υπολογισμός επόμενης κατάστασης

Ενημέρωση Τρέχουσας Κατάστασης

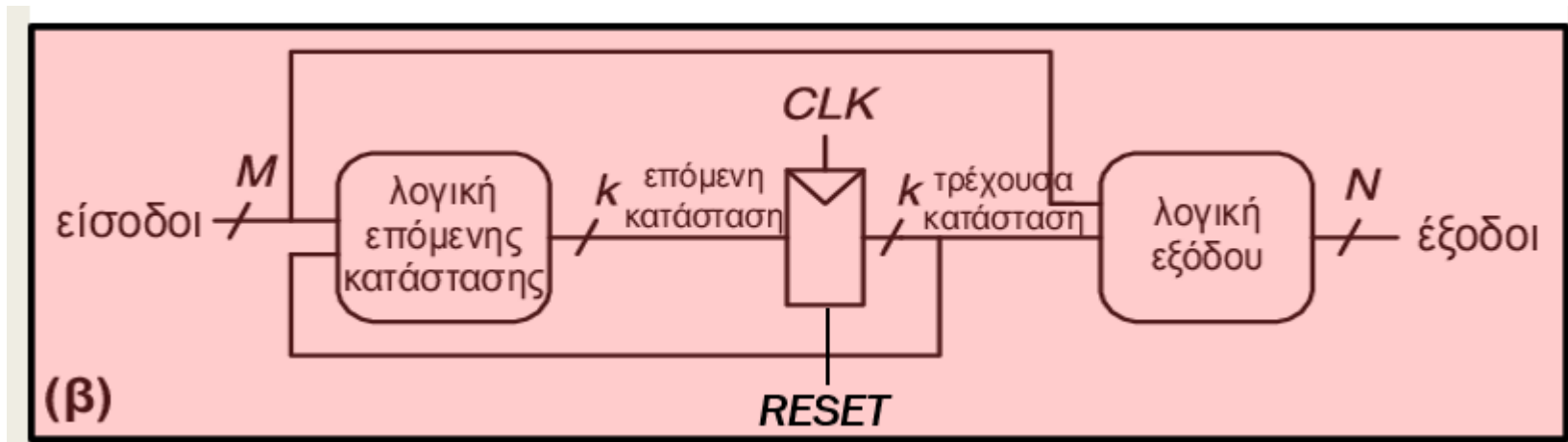
B

Μετρώ δευτερόλεπτα

Υπολογισμός εξόδου

4^η Εργαστηριακή Άσκηση

Ανάλυση άσκησης



4^η Εργαστηριακή Άσκηση

ΠΡΟΧΩΡΗΣΤΕ ΣΤΗΝ ΑΣΚΗΣΗ



4^η Εργαστηριακή Άσκηση

Αρχιτεκτονική (1/3) – Νέο Ρολόι (Περίοδος = 1 sec)

Αρχιτεκτονική



```
new_clk_counts<=clk_counts+1 when clk_counts<100000000 else 0;
```

```
counts_100M : process (clk, reset) is  
variable clk_ticks : integer;
```

```
begin
```

```
if reset = '1' then
```

```
    clk_counts<=0;
```

```
elsif rising_edge(clk) then
```

```
    clk_counts<=new_clk_counts;
```

```
end if; --reset
```

```
end process counts_100M;
```

```
clk_one_sec<='1' when clk_counts=100000000 else '0';
```

4^η Εργαστηριακή Άσκηση

Αρχιτεκτονική (2/3) – Tick Counter

Αρχιτεκτονική →

```
process(clk_one_sec) is
begin

if (clk_one_sec='1') then
  if (direction='1' and sec_counts<9) then
    new_sec_counts<= sec_counts+1;
  elsif (direction='0' and sec_counts>0) then
    new_sec_counts<= sec_counts-1;
  elsif (direction='0' and sec_counts<=0) then
    new_sec_counts<= "1001";
  elsif (direction='1' and sec_counts>=9) then
    new_sec_counts<="0000";
  else
    new_sec_counts<="0000";
  end if;
else
  new_sec_counts<=sec_counts;
end if;

end process;
```

```
count_seconds: process (clk, reset) is
begin

if (reset='1') then
  sec_counts<=(others=>'0');
elsif rising_edge(clk) then
  sec_counts<=new_sec_counts;
end if; --reset

end process count_seconds;
```

4^η Εργαστηριακή Άσκηση

Αρχιτεκτονική (3/3) – Output signals

Αρχιτεκτονική



```
led_result<=std_logic_vector(sec_counts);
```

```
counts_digit_values: process (sec_counts) begin
```

```
case sec_counts is
```

```
  when X"0" => seven_segment <="0111111"; -- 0
```

```
  when X"1" => seven_segment <="0000110"; -- 1
```

```
  when X"2" => seven_segment <="1011011"; -- 2
```

```
  when X"3" => seven_segment <="1001111"; -- 3
```

```
  when X"4" => seven_segment <="1100110"; -- 4
```

```
  when X"5" => seven_segment <="1101101"; -- 5
```

```
  when X"6" => seven_segment <="1111101"; -- 6
```

```
  when X"7" => seven_segment <="0000111"; -- 7
```

```
  when X"8" => seven_segment <="1111111"; -- 8
```

```
  when X"9" => seven_segment <="1101111"; -- 9
```

```
  when others => seven_segment <="0000000";
```

```
end case;
```

```
end process counts_digit_values;
```

```
digit_selection_out<=digit_selection_in;
```

4^η Εργαστηριακή Άσκηση

Constraints (1/2) – CLK + Switches + Leds

```
# CLK - Zedboard 100MHz oscillator
set_property -dict { PACKAGE_PIN Y9 IOSTANDARD LVCMOS33 } [get_ports {clk}]
```

```
#####
# On-board Slide Switches #
#####
```

```
set_property -dict { PACKAGE_PIN M15 IOSTANDARD LVCMOS33 } [get_ports { digit_selection_in }];
set_property -dict { PACKAGE_PIN H17 IOSTANDARD LVCMOS33 } [get_ports { reset }];
set_property -dict { PACKAGE_PIN F22 IOSTANDARD LVCMOS33 } [get_ports { direction }];
```

```
#####
# On-board LEDS #
#####
```

```
set_property -dict { PACKAGE_PIN T22 IOSTANDARD LVCMOS33 } [get_ports { led_result[0] }];
set_property -dict { PACKAGE_PIN T21 IOSTANDARD LVCMOS33 } [get_ports { led_result[1] }];
set_property -dict { PACKAGE_PIN U22 IOSTANDARD LVCMOS33 } [get_ports { led_result[2] }];
set_property -dict { PACKAGE_PIN U21 IOSTANDARD LVCMOS33 } [get_ports { led_result[3] }];
```

Constraints



4^η Εργαστηριακή Άσκηση

Constraints (1/2) – Pmod

```
#####  
# PmodSSO          #  
#####  
  
set_property -dict { PACKAGE_PIN Y11  IOSTANDARD LVCMOS33 } [get_ports { seven_segment[0] }];  
set_property -dict { PACKAGE_PIN AA11 IOSTANDARD LVCMOS33 } [get_ports { seven_segment[1] }];  
set_property -dict { PACKAGE_PIN Y10  IOSTANDARD LVCMOS33 } [get_ports { seven_segment[2] }];  
set_property -dict { PACKAGE_PIN AA9   IOSTANDARD LVCMOS33 } [get_ports { seven_segment[3] }];  
set_property -dict { PACKAGE_PIN W12  IOSTANDARD LVCMOS33 } [get_ports { seven_segment[4] }];  
set_property -dict { PACKAGE_PIN W11  IOSTANDARD LVCMOS33 } [get_ports { seven_segment[5] }];  
set_property -dict { PACKAGE_PIN V10  IOSTANDARD LVCMOS33 } [get_ports { seven_segment[6] }];  
  
set_property -dict { PACKAGE_PIN W8   IOSTANDARD LVCMOS33 } [get_ports { digit_selection_out }];  
  
#####  
##ZedBoard Timing Constraints  
#####  
# define clock and period  
create_clock -period 10 -name CLK -waveform {0.000 5.000} [get_ports {clk}]
```

Constraints



4^η Εργαστηριακή Άσκηση

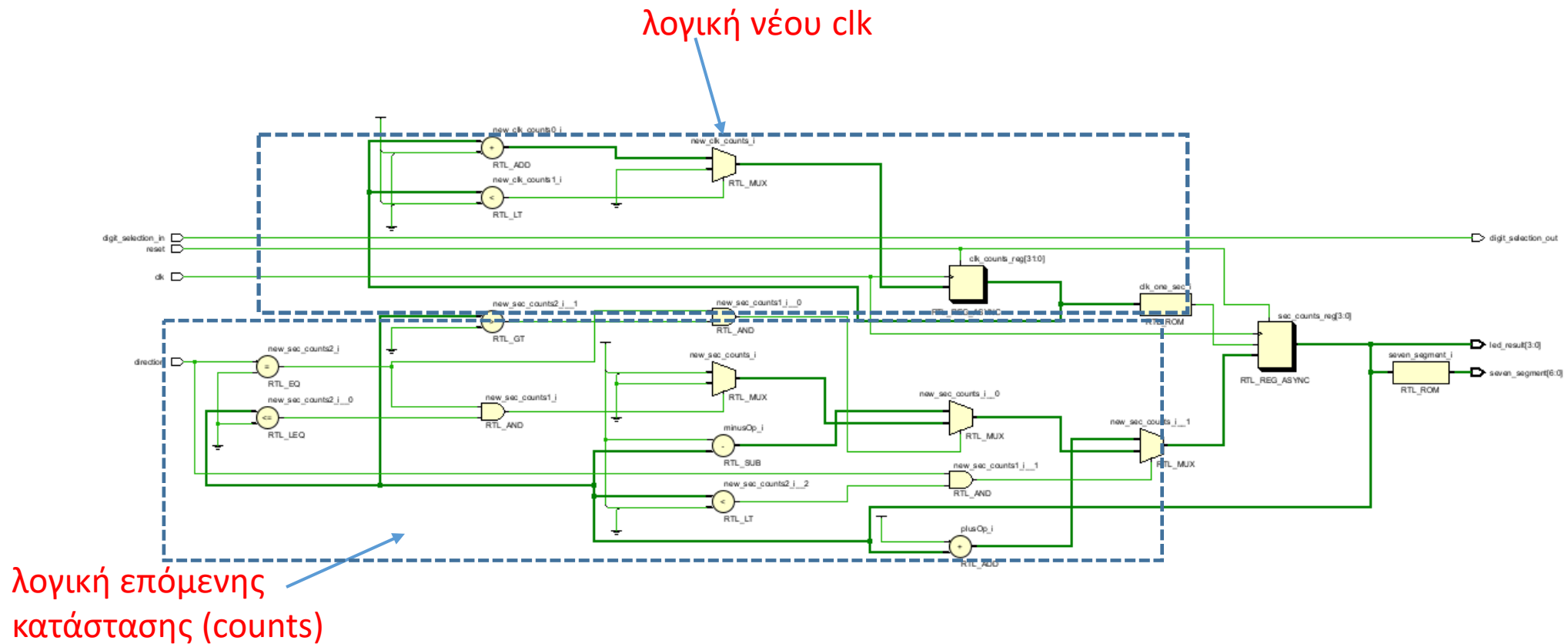
Pmod Manual

Manual Pmod

<https://reference.digilentinc.com/reference/pmod/pmodssd/reference-manual>

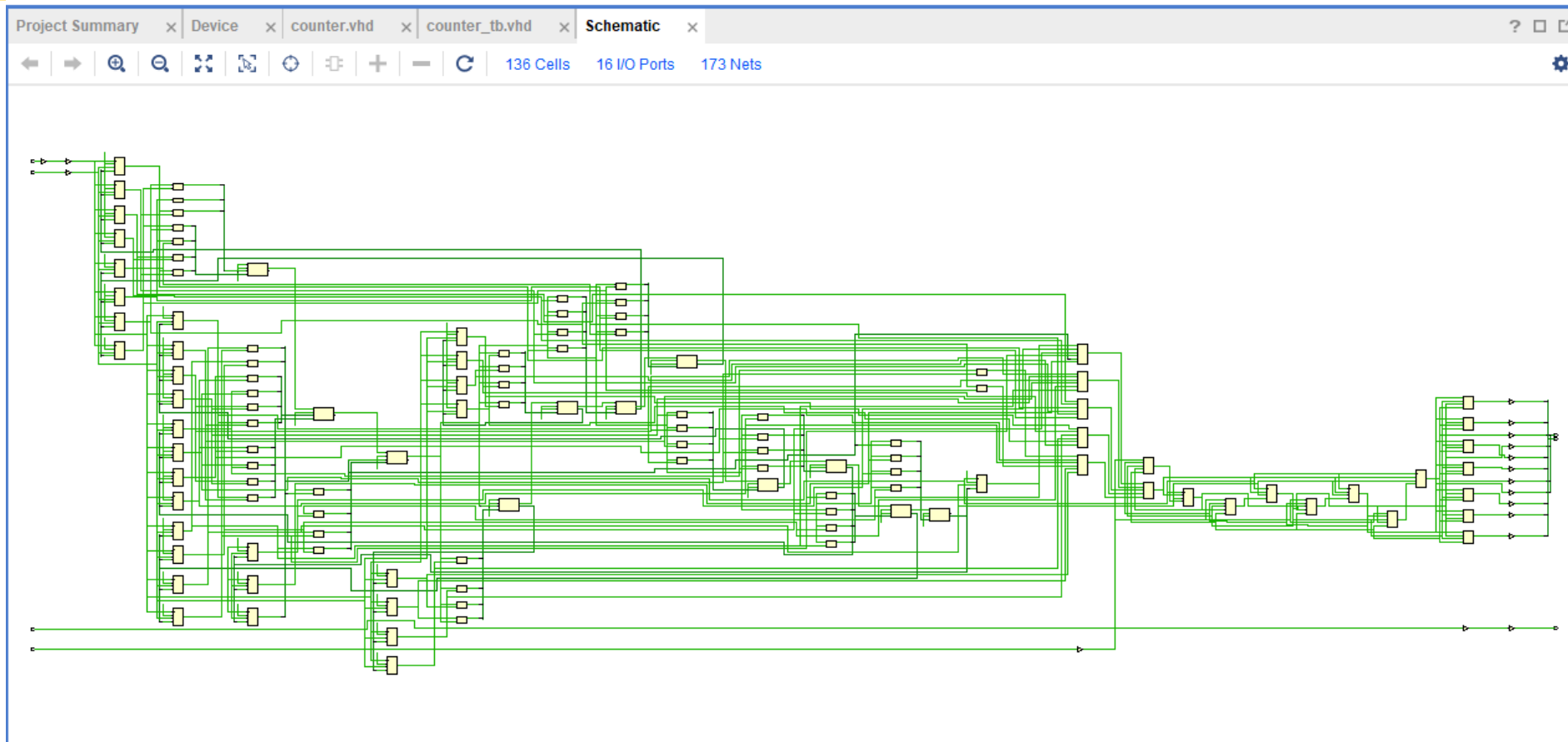
4^η Εργαστηριακή Άσκηση

RTL Design



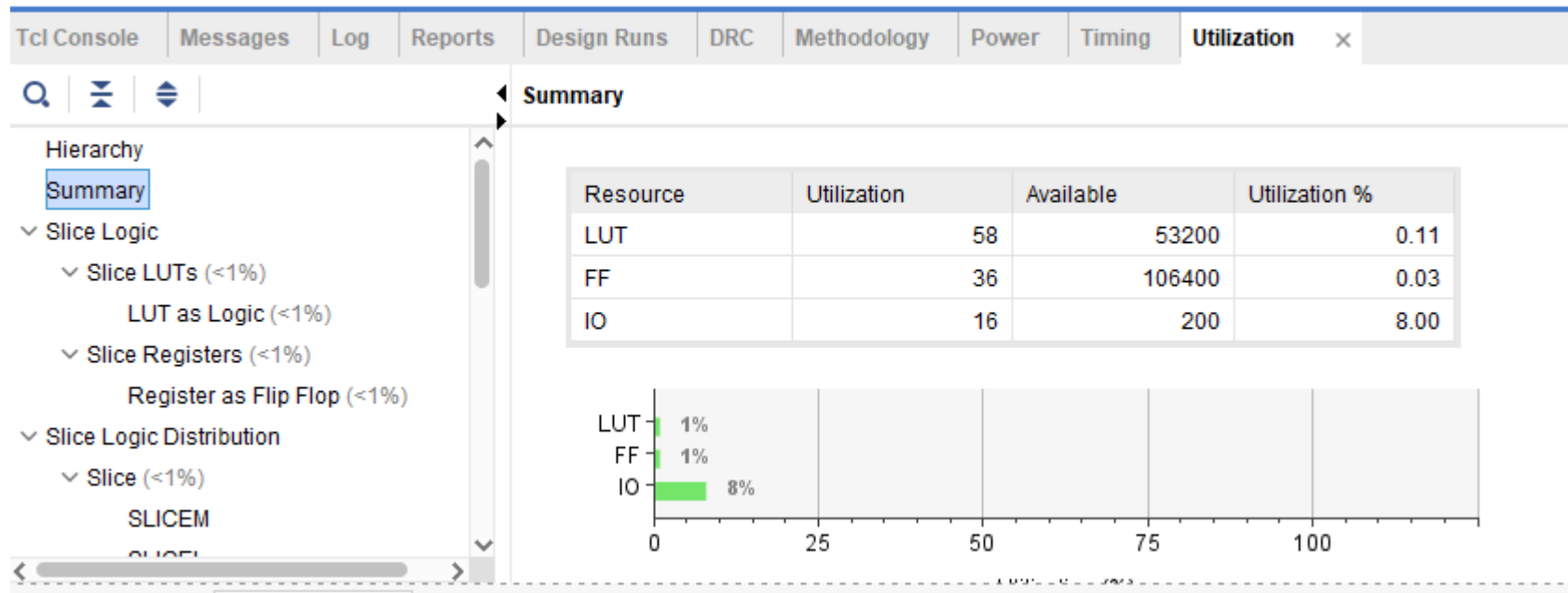
4^η Εργαστηριακή Άσκηση

Synthesis/Implementation – Schematic



4^η Εργαστηριακή Άσκηση

Implementation – Report Utilization



Και από Project Summary

4^η Εργαστηριακή Άσκηση

Implementation – Timing Reports (1/4)

Menu Reports->Timing-> Report Timing Summary

ή

Open Implemented Design->Report Timing Summary

The screenshot shows the 'Design Timing Summary' report in a software interface. The report is organized into three columns: Setup, Hold, and Pulse Width. The data is as follows:

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 3,913 ns	Worst Hold Slack (WHS): 0,287 ns	Worst Pulse Width Slack (WPWS): 4,500 ns
Total Negative Slack (TNS): 0,000 ns	Total Hold Slack (THS): 0,000 ns	Total Pulse Width Negative Slack (TPWS): 0,000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 40	Total Number of Endpoints: 40	Total Number of Endpoints: 37

All user specified timing constraints are met.

4^η Εργαστηριακή Άσκηση

Implementation – Timing Reports (2/4)

The screenshot displays the Xilinx Vivado interface. The top window shows a schematic diagram of a circuit with various components and connections. The bottom window shows the Timing Report for Intra-Clock Paths - CLK - Setup. The report table is as follows:

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Exception	Clock Uncertainty
Path 1	3.913	13	33	clk_counts_reg[8]C	clk_counts_reg[29]D	6.137	3.084	3.053	10.000	CLK	CLK		0.035
Path 2	3.921	13	33	clk_counts_reg[8]C	clk_counts_reg[31]D	6.129	3.076	3.053	10.000	CLK	CLK		0.035
Path 3	3.997	13	33	clk_counts_reg[8]C	clk_counts_reg[30]D	6.053	3.000	3.053	10.000	CLK	CLK		0.035
Path 4	4.017	13	33	clk_counts_reg[8]C	clk_counts_reg[28]D	6.033	2.980	3.053	10.000	CLK	CLK		0.035
Path 5	4.030	12	33	clk_counts_reg[8]C	clk_counts_reg[25]D	6.020	2.967	3.053	10.000	CLK	CLK		0.035
Path 6	4.038	12	33	clk_counts_reg[8]C	clk_counts_reg[27]D	6.012	2.959	3.053	10.000	CLK	CLK		0.035
Path 7	4.114	12	33	clk_counts_reg[8]C	clk_counts_reg[26]D	5.936	2.883	3.053	10.000	CLK	CLK		0.035
Path 8	4.134	12	33	clk_counts_reg[8]C	clk_counts_reg[24]D	5.916	2.863	3.053	10.000	CLK	CLK		0.035
Path 9	4.147	11	33	clk_counts_reg[8]C	clk_counts_reg[21]D	5.903	2.850	3.053	10.000	CLK	CLK		0.035
Path 10	4.155	11	33	clk_counts_reg[8]C	clk_counts_reg[23]D	5.895	2.842	3.053	10.000	CLK	CLK		0.035

Setup Time:

Αναφέρεται στις αργές διαδρομές (καθυστέρηση διάδοσης)

4^η Εργαστηριακή Άσκηση

Implementation – Timing Reports (3/4)

The screenshot displays the Xilinx Vivado IDE. The top window shows a schematic diagram of a counter circuit with various registers (clk_counts_reg) and LUTs. The bottom window shows the Timing Report for Intra-Clock Paths - CLK - Hold.

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Exception	Clock Uncertainty
Path 11	0.287	2	2	clk_counts_reg[7]C	clk_counts_reg[7]D	0.421	0.273	0.148	0.000	CLK	CLK		0.000
Path 12	0.288	2	2	clk_counts_reg[3]C	clk_counts_reg[3]D	0.422	0.273	0.149	0.000	CLK	CLK		0.000
Path 13	0.288	2	3	clk_counts_reg[11]C	clk_counts_reg[11]D	0.422	0.273	0.149	0.000	CLK	CLK		0.000
Path 14	0.288	2	4	clk_counts_reg[19]C	clk_counts_reg[19]D	0.422	0.273	0.149	0.000	CLK	CLK		0.000
Path 15	0.300	2	4	clk_counts_reg[23]C	clk_counts_reg[23]D	0.434	0.273	0.161	0.000	CLK	CLK		0.000
Path 16	0.300	2	4	clk_counts_reg[27]C	clk_counts_reg[27]D	0.434	0.273	0.161	0.000	CLK	CLK		0.000
Path 17	0.300	2	4	clk_counts_reg[15]C	clk_counts_reg[15]D	0.434	0.273	0.161	0.000	CLK	CLK		0.000
Path 18	0.300	2	4	clk_counts_reg[31]C	clk_counts_reg[31]D	0.434	0.273	0.161	0.000	CLK	CLK		0.000
Path 19	0.312	1	12	sec_counts_reg[1]C	sec_counts_reg[1]D	0.419	0.230	0.189	0.000	CLK	CLK		0.000
Path 20	0.314	1	12	sec_counts_reg[1]C	sec_counts_reg[3]D	0.421	0.231	0.190	0.000	CLK	CLK		0.000

Hold Time:

Αναφέρεται στις γρήγορες διαδρομές (καθυστέρηση μόλυνσης)

4^η Εργαστηριακή Άσκηση

Implementation – Timing Reports (4/4)

TCL Console>*report_timing_summary -datasheet*

The screenshot shows the TCL Console interface with a menu bar (Messages, Log, Reports, Design Runs, DRC, Methodology, Power, Timing, Utilization) and a toolbar. The main content area displays the output of the `report_timing_summary -datasheet` command. The output is titled "Combinational Delays" and contains a table with the following data:

From Port	To Port	Max Delay (ns)	Process Corner	Min Delay (ns)	Process Corner
digit_selection_in	digit_selection_out	10.817	SLOW	3.770	FAST

Below the table, the text "Setup between Clocks" is visible. A red arrow points from the right side of the slide to the value 10.817 in the table.

Προσοχή