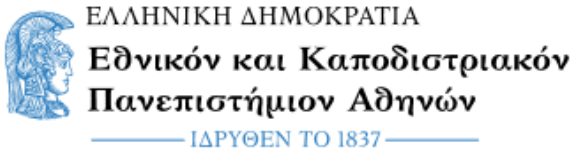


ΣΧΟΛΗ ΘΕΤΙΚΩΝ ΕΠΙΣΤΗΜΩΝ

ΔΠΜΣ Space Technologies, Applications and seRvices (STAR)

M806 Space Data Systems

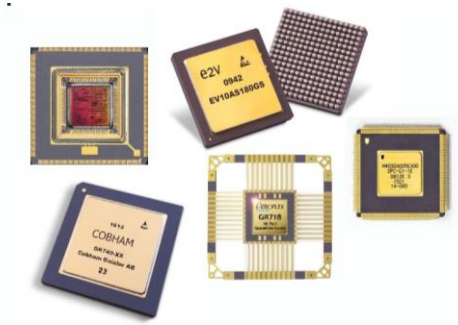
ECSS standards for ASIC, FPGA and IP Core Engineering and Product Quality Assurance

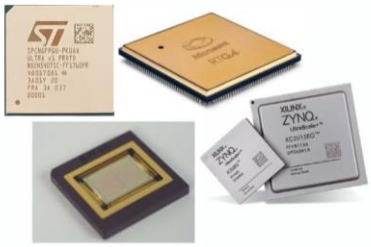
Ακαδημαϊκό Έτος 2023-2024

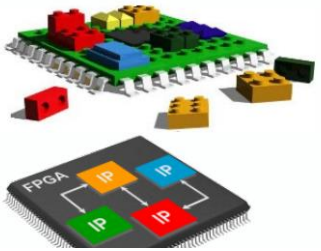
Νεκτάριος Κρανίτης

ECSS standards for ASIC, FPGA and IP Cores

- Applicable in R&D activities and projects
- Setting high-level requirements for successful engineering and product assurance of:
  - **ASICs** (Application Specific Integrated Circuits)
    - Can be digital, mixed-signal or analog
    - Microprocessors, DSPs, GPUs are special “general purpose” group of ASICs
  - **FPGAs** (Field Programmable Gate Arrays)
    - Can embed “processing” cores (use SW to operate!)
  - **IP Cores** (Intellectual Property Cores)
    - “Soft” models of ICs
    - Reused as “building blocks” to develop ASICs and FPGAs faster





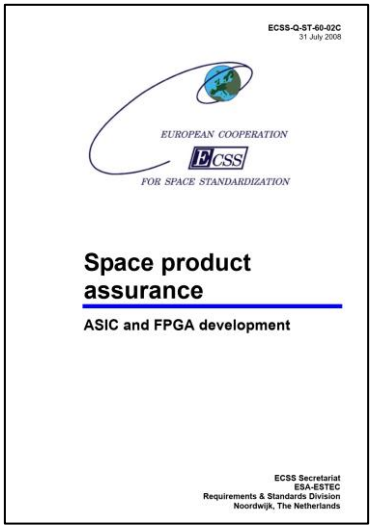


Credit: ESA

ECSS standards for ASIC, FPGA and IP Cores

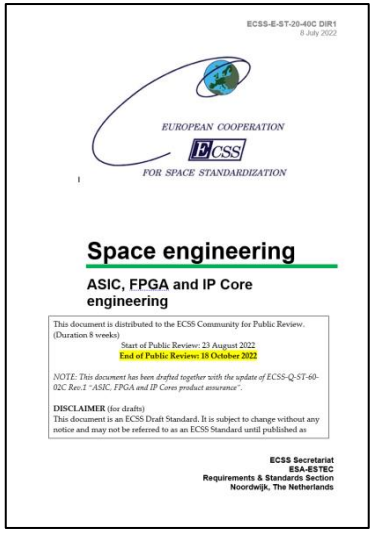
2018

- ECSS-Q-HB-60-02C Space Product Assurance: ASIC and FPGA development

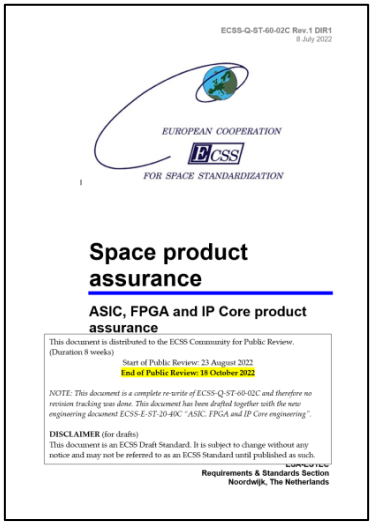


2023

- ECSS-**E**-ST-20-40 ASIC, FPGA and IP Core **engineering**
- ECSS-**Q**-ST-60-02C Rev.1 ASIC, FPGA and IP Core **product assurance**



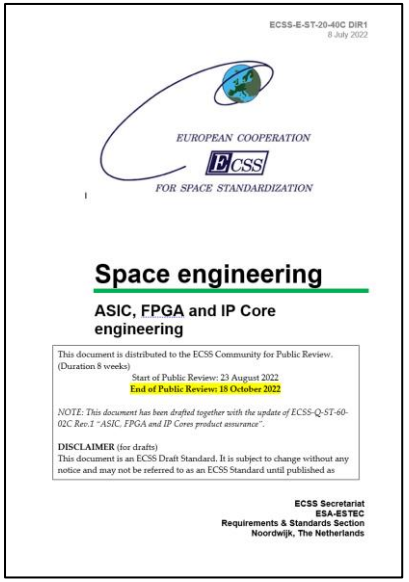
Separation of **engineering** (in E-ST-20-40) versus **product assurance** requirements (in Q-ST-60-02C Rev.1)



Credit: ESA

New ECSS standards

- **ECSS-E-ST-20-40 - Engineering**
  - Starting points:
    - all chapters and requirements of old ECSS-Q-ST-60-02C chapter 5 (ASIC and FPGA engineering)
    - all requests for changes gathered from industry and ESA experts, reviewed item by item, improving/adding/superseding many requirements, having as reference a generic development flow that admits variations, different types of DEVICES, and 2 main criticality levels


ECSS-E-ST-20-40C DIR1
8 July 2022

EUROPEAN COOPERATION FOR SPACE STANDARDIZATION

Space engineering

ASIC, FPGA and IP Core engineering

This document is distributed to the ECSS Community for Public Review. (Duration 8 weeks)

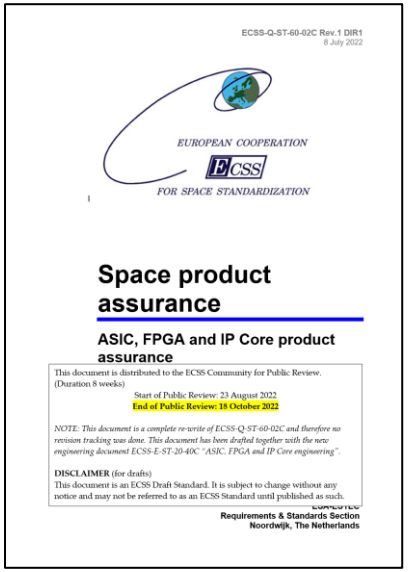
Start of Public Review: 23 August 2022
End of Public Review: 18 October 2022

NOTE: This document has been drafted together with the update of ECSS-Q-ST-60-02C Rev.1 "ASIC, FPGA and IP Cores product assurance".

DISCLAIMER (for drafts)
This document is an ECSS Draft Standard. It is subject to change without any notice and may not be referred to as an ECSS Standard until published as

ECSS Secretariat
ESA-ESTEC
Requirements & Standards Section
Noordwijk, The Netherlands

- **ECSS-Q-ST-60-02C Rev.1 – Product Assurance**
  - Inspired from Q-ST-80 (SW Product Assurance)
  - But adapted to DEVICE (IC and IP) developments, as PA complement to the new E-ST-20-40.
  - Seeking compliance to ECSS-Q/M branches


ECSS-Q-ST-60-02C Rev.1 DIR1
8 July 2022

EUROPEAN COOPERATION FOR SPACE STANDARDIZATION

Space product assurance

ASIC, FPGA and IP Core product assurance

This document is distributed to the ECSS Community for Public Review. (Duration 8 weeks)

Start of Public Review: 23 August 2022
End of Public Review: 18 October 2022

NOTE: This document is a complete re-write of ECSS-Q-ST-60-02C and therefore no revision tracking was done. This document has been drafted together with the new engineering document ECSS-E-ST-20-40C "ASIC, FPGA and IP Core engineering".

DISCLAIMER (for drafts)
This document is an ECSS Draft Standard. It is subject to change without any notice and may not be referred to as an ECSS Standard until published as such.

Requirements & Standards Section
Noordwijk, The Netherlands

Credit: ESA

Separating Engineering from PA requirements

- Requirement overlaps between E-ST-20-40 and Q-ST-60-02 Rev.1 as Engineering/PA borderline is at times blurry
- Same or similar things are called sometimes different names, and sometimes same words can have different meanings in the context of different standards
  - e.g., “verification”, “validation” or “qualified”, which needs context words : “ECSS PA qualified” vs. “ESCC qualified” vs. “MIL QML-V qualified”…
- Q-60-02C Rev.1 adheres strictly to other applicable ECSS Q and M standards, using their terminology
- E-ST-20-40 uses terminology that is widely used by ASIC and FPGA engineers

- Both standards shall be applied, in parallel, and supervised by:
  - an ASIC/FPGA/IP **Engineer** (e.g., ESA technical officer or expert) and
  - a Product Assurance responsible
- Customer “DEVICE acceptance” as “fully verified and validated” (E-20-40) and “PA qualified” (Q-60-02C Rev.1)” is subject to successful final reviews as defined in both standards

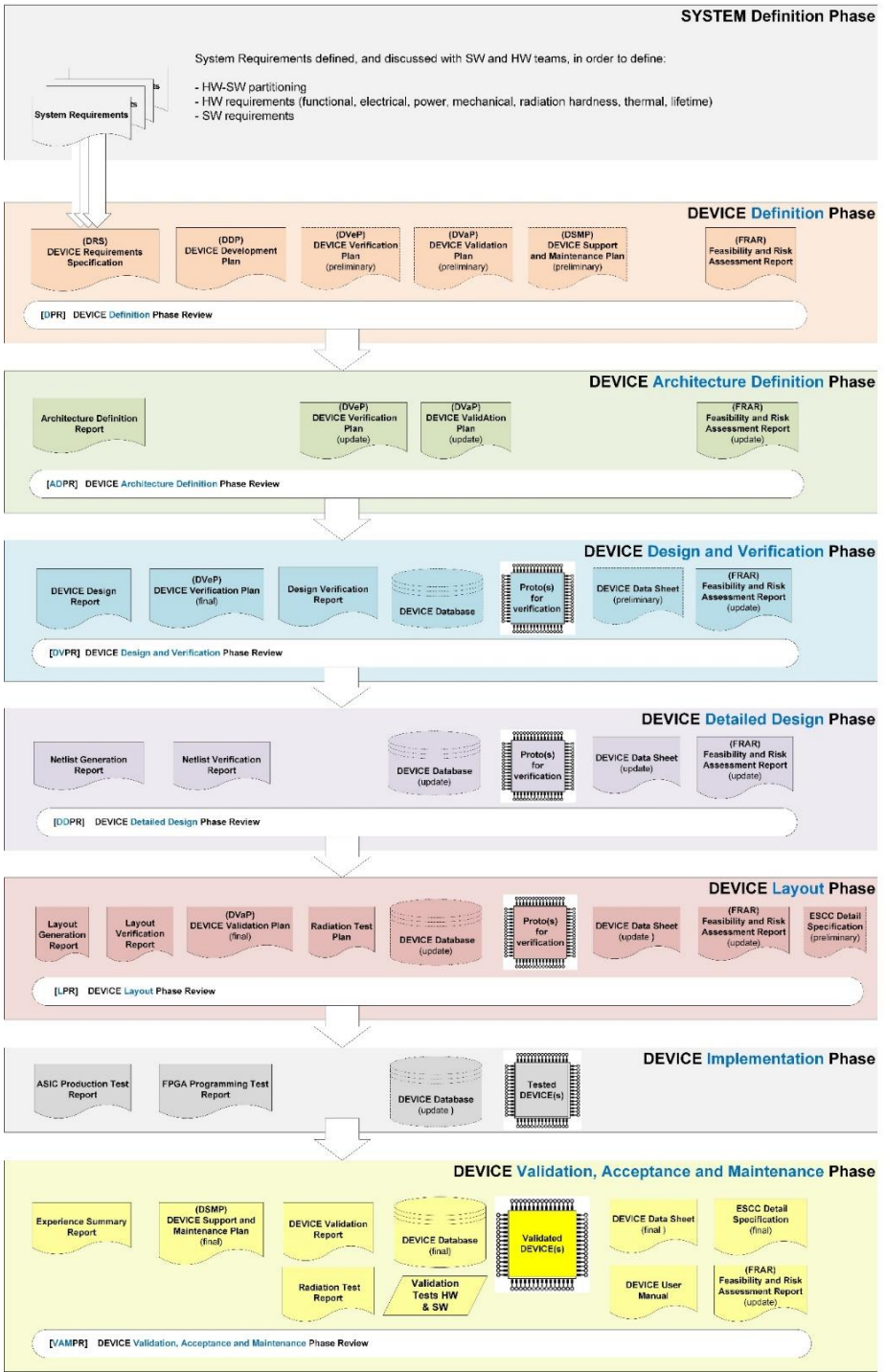
Credit: ESA

Devices and IP Cores according to ECSS-E-ST-20-40

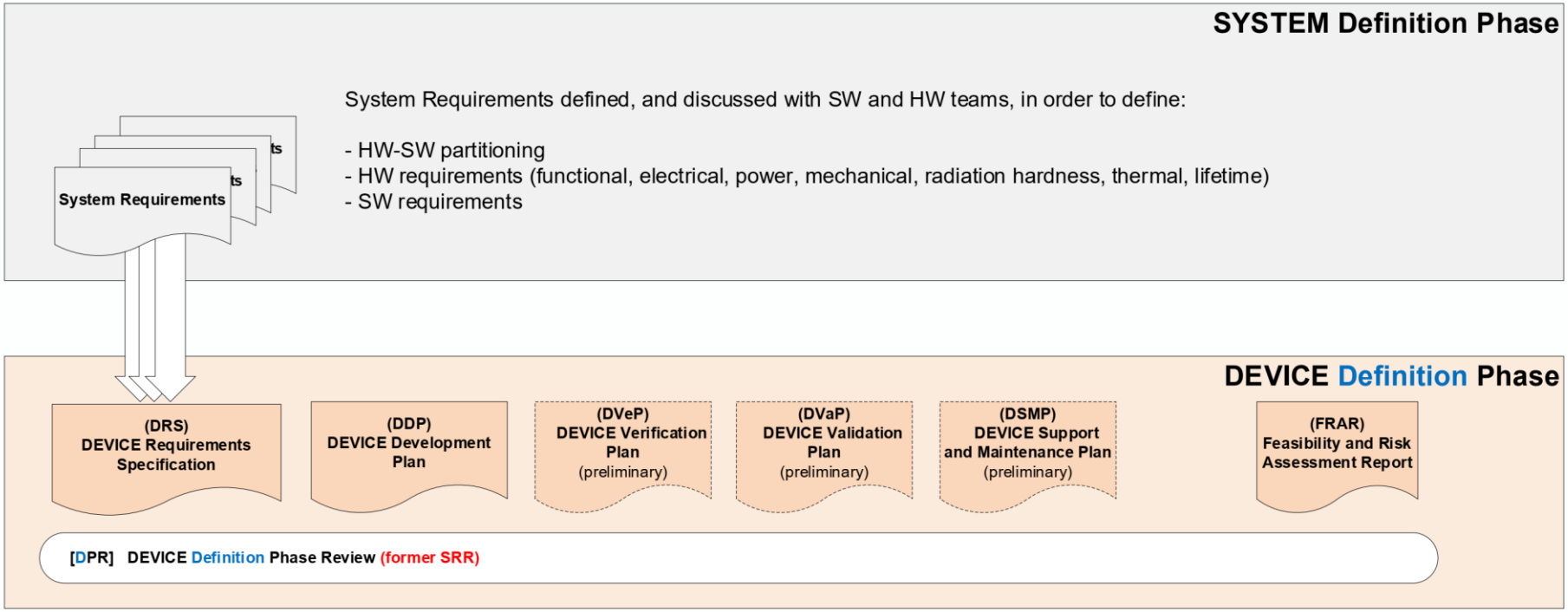
- Device:
  - Integrated Circuit (IC) or an IP Core
  - A DEVICE can be a digital, analog or mixed-signal ASIC, programmed FPGA, blank FPGA, microprocessor, and model of IC function conceived for reuse as IP Core
- IP Core:
  - IC design element that implements a self-standing function or group of functions for which ownership rights exist and is developed for reuse and released with comprehensive verification, validation and documentation
    - Can be acquired by a customer, for a given price and under an owner-defined license agreement specifying the customer's acquired rights
    - Can be supplied as an HDL model, as a synthesizable VHDL code or gate-level netlist, and with the essential complementary documentation that allows the customer to successfully integrate and use it in a system for example User's manual and verification files.
    - Can be analog functions provided by DEVICE technology providers as macrocells
    - In contrast with Building Blocks, IP Cores have gone through comprehensive verification, validation and documentation intended for reuse of third parties
    - Referred as *hard IPs* if they are already placed and routed for one specific IC technology

ECSS-E-ST-20-40

- Generic development flow
- Involves going through a flow of several phases which encompass several engineering steps



ECSS-E-ST-20-40 Phases, Reviews and Outputs



- **DEVICE Definition Phase**:
  - Establish a DEVICE Requirements Specification (DRS) that results from carefully flowing down the requirements of system(s) where DEVICE is used, ensuring good traceability between the DEVICE and the System Requirements
  - Establish a DEVICE Development Plan (DDP) that defines development flow, indicating the resources and schedules
  - Feasibility and Risk Assessment (FRAR) report is an important part of this initial DEVICE Definition Phase, and is revised in the following phases in order to minimize risks

DEVICE Development Plan (DDP)

- **Purpose**: implement the proposed development strategy by identifying:
  - all phases of the DEVICE development with the major activities therein
  - the project external interfaces and constraints
  - the design flow
  - resources such as equipment, software and personnel
  - the allocation of responsibilities
  - outputs produced
  - a schedule with milestones, decision points, type and number of design reviews
- Include versions & platforms of tools, including design kits or specific tools, and a statement for availability of each tool at each site for every development phase
- Define the DEVICE development flow, including a brief description of the phases, the main tasks of each phase and any variations with respect to the generic flow
- Include a description of inputs and outputs of each phase indicating their format
- And many more…

Feasibility and Risk Assessment (FRAR)

- **Purpose**:
  - To document the conclusions of the evaluation of the feasibility of the development as defined in the DRS and the DDP, considering the available technical and human resources
  - To document the conclusions of the assessment of the risks and contingency plans and their impact in the DDP

DEVICE Verification Plan (DVeP)

- **Purpose**: define strategy to **prove that all DRS requirements is met**
  - using different verification methods
  - starting from higher-level DEVICE models, reviewed at DEVICE Design and Verification Phase Review
  - down-to the gate level DEVICE database and the layout, reviewed at DEVICE Detailed Design and Layout Phase Reviews, used for manufacturing or programming the DEVICE
- Include a description of verification environment for the methods applied, including analysis & simulation tools and HW-SW test platforms used
- Include type of verification method applied for each requirement, including a matrix for traceability of their execution and results obtained
  - analysis (A), design review (DR), simulation (S), prototype HW tests (T) or inspection (I)
- Define strategy to verify that chosen radiation hardening concept is applied meeting expected results
- Define code and functional coverage verification strategy, indicating which types of coverage and which target figures/margins are applicable
- Specify which tools are used for code and functional coverage verification
- And many more…

DEVICE Validation Plan (DVaP)

- **Purpose**: define strategy, based on tests & measurements in a representative system, that **proves final manufactured/programmed DEVICE performs and behaves as expected in intended system, operational environment and application scenarios**
- Define the tests and measurements performed, including a matrix for traceability of their execution and the results obtained
- Include a description of HW & SW test set-up representative of intended system environment that is used to perform the validation tests and measurements
  - E.g., validation test set-up can include ad-hoc DEVICE test boards or engineering model system boards and dedicated test software.
- Define the operating modes and test conditions of the DEVICE under validation
- Include validation strategy of IP Cores integrated in the DEVICE
- And many more…

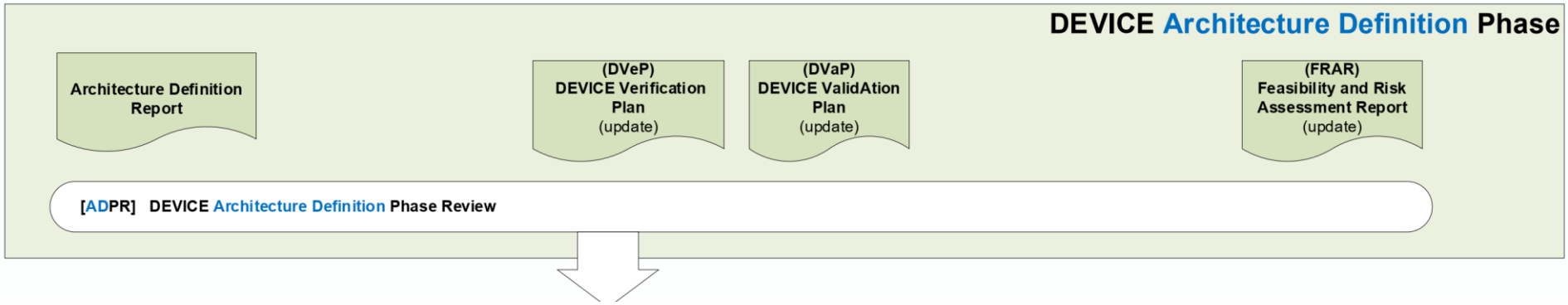
Verification vs Validation

- Verification: DEVICE was designed right
  - checking compliance with the requirements
- Validation: DEVICE manufactured/programmed is the right design
  - Checking compliance with the need
  - The DEVICE is able to accomplish its intended use

DEVICE Support and Maintenance Plan (DSMP)

- **Purpose**: define what resources and during which time frame, are provided by supplier to customer in order to:
  - Help DEVICE users with any problems encountered during inclusion and its use in its intended system due to problems in DEVICE itself or its documentation
  - Facilitate modifications or future developments of new DEVICEs which can reuse infrastructure and same outputs generated during present development

ECSS-E-ST-20-40 Phases, Reviews and Outputs

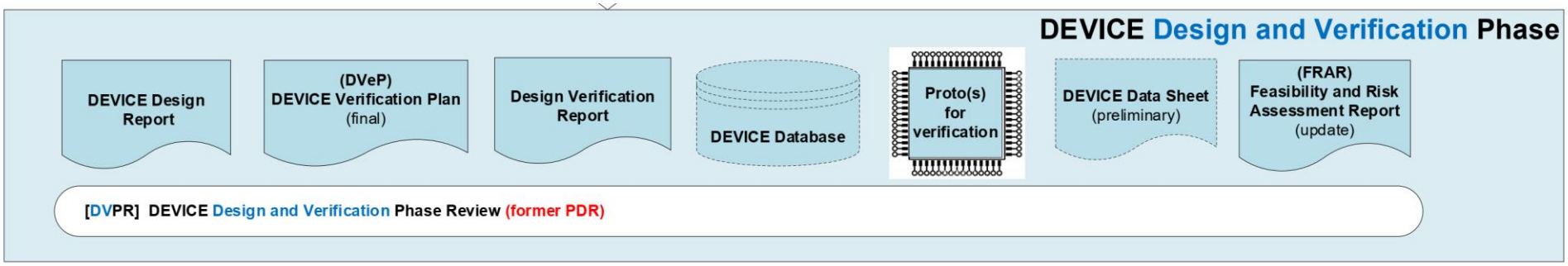


- **DEVICE Architecture Definition Phase**:
  - Define the architecture of the DEVICE design in terms of:
    - its main functional blocks
    - hierarchies and dependencies of these blocks
    - their interfaces and how they interconnect
  - Objective: facilitate modular and detailed design of all blocks and their integration in the following phases

Architecture Definition Report (ADR)

- **Purpose:** define architecture of the DEVICE design in terms of its main functional blocks, hierarchies and dependencies of these blocks, their interfaces and how they interconnect
- Include a subdivision of DEVICE into its fundamental functions or blocks, identifying and documenting their main interfaces, functionalities, performances, hierarchical dependencies and flowing down all the requirements for each block
- Include a description of communication and data flow between main functional blocks and data paths
- Include definition of the architecture down to the level needed for the following DEVICE Design and Verification Phase
- Include suitable algorithms and circuit schemes including their parameters to implement the identified functions
- Identify which circuit architecture elements are introduced to meet
  - test requirements
  - radiation hardness requirements
- And many more…

ECSS-E-ST-20-40 Phases, Reviews and Outputs

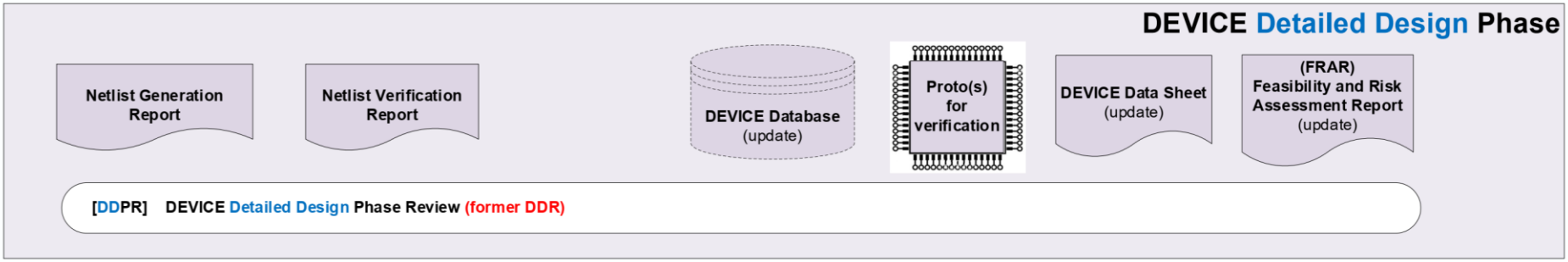


- **DEVICE Design and Verification Phase**:
  - Create the first DEVICE models and their verification environment
    - These models are part of the DEVICE Database
  - DEVICE model creation and its verification is documented in DEVICE Design Report and the Design Verification Report respectively
  - A preliminary DEVICE Data Sheet is prepared
  - Phase concludes with DEVICE Design and Verification Phase Review
    - Secure that everything is ready for the DEVICE Detailed Design Phase

DEVICE Data Sheet (DDS)

- **Purpose:** provide DEVICE users with all technical data needed to correctly and reliably use DEVICE for intended applications and system environments
  - DDS explains **what** the DEVICE does and **how** it can be used.
- Contains summary of DEVICE functionality, block diagram and short list of main features
  - E.g., key functions, timing, voltage, thermal and radiation operating ranges
- Contains a DEVICE system overview and a description of how to use the DEVICE in a representative system environment
- Contains a full functionality description including all operating modes
- Specifies in detail:
  - Internal registers or memory maps used to define functional operation
  - Input pins putting the DEVICE into different operating modes
  - Both test and nominal functions
- Explains all test modes functions, indicating which pins and internal registers and memories are controlling them and providing external observability
- If internal functions need special start-up sequences to put DEVICE in a correct operating mode, DDS shall explain those start up sequences and specify any internal registers or output pins used to do health checks of the correct status of the DEVICE
- And many more…

ECSS-E-ST-20-40 Phases, Reviews and Outputs



- **DEVICE Detailed Design Phase**:
  - DEVICE design is translated into a structural description at the level of elementary cells of the selected technology and cell library: **pre-layout netlist**
  - Additional information is generated for subsequent development phases
    - Layout constraints, floor-planning, Production Tests programs and a detailed pin description
  - For digital designs, the above-mentioned design description is the technology specific gate-level pre-layout netlist normally obtained by synthesis tools
  - For analog designs, it is a verified sized transistor-level netlist
    - In many analog designs, there is no separation between circuit netlist design and layout.
  - Meeting DEVICE timing, occupancy and power targets sometimes can need performing iterations between netlist generation and layout generation

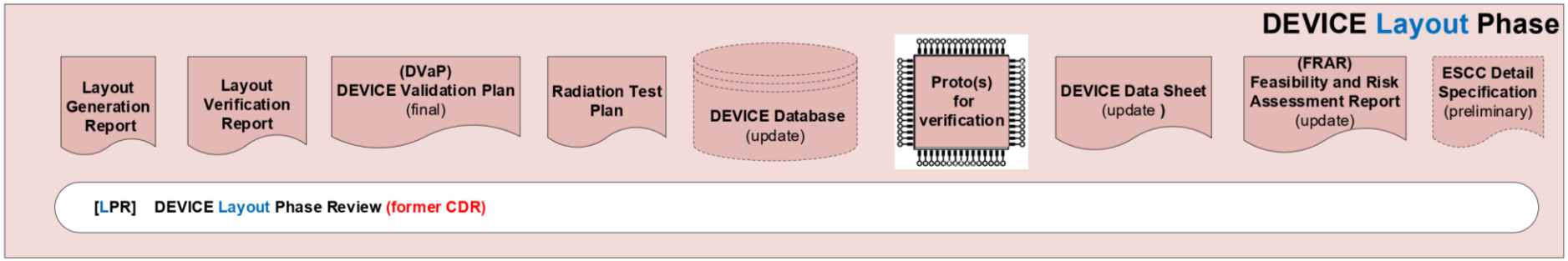
Netlist Generation

- Choose and implement pre-layout netlist generation with selected tool options and constraints
  - E.g. script variables & commands to control timing, area, power, types of library cells used or different synthesis modes for complex DEVICES
- Clock, reset and other signals with specific buffering and delay-controlled distribution with high fan-out shall be implemented using available netlist generation resources
- DFT and Production Tests requirements shall be implemented
- Radiation hardness concept shall be implemented
  - E.g., TMR, safe state machines or error detection and correction
- Floorplan shall be defined or refined if already existing
- I/O buffers shall be confirmed and implemented
- Implement design parameter centring based on simulations, allowing margins that account for final layout and process variations, to maximize yield
- Justify and document any library cells selections
  - E.g. some cells can be excluded due to their weaker radiation performance
- Describe any logic cells that were specially developed for the DEVICE

Netlist Generation (cont.)

- Describe any Design-For-Manufacturability strategies applied
- Specify and justify the use of any black-boxes in the netlist
- Document all constraints applied during netlist generation
- Utilization of available resources shall be determined and documented
- Specify configuration and netlist generation constraints applied to IP Cores used in the DEVICE netlist
- Deviations from IP Core provider recommendations for netlist generation of IP Core shall be documented and justified
- Document any applied derating factors
- Document any applied margins
- Influences from layout such as cross talk and matching shall be accounted for during the detail design work
- Document how parasitic effects are dealt with

ECSS-E-ST-20-40 Phases, Reviews and Outputs

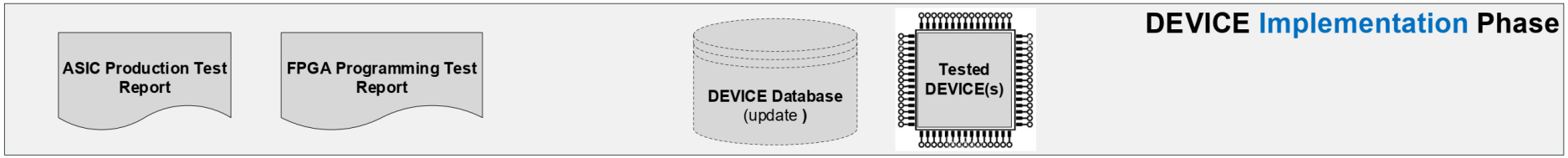


- **DEVICE Layout Phase**:
  - Generate structural description of DEVICE at the level of elementary cells of the selected technology and libraries creating a Placed and Routed (P&R) model of netlist and all complementary files needed to manufacture/program the DEVICE

Layout Generation

- Floorplan of DEVICE shall be finalized
- Core and I/O-pad ring power distribution shall be generated
- Test pads, if needed, shall be generated
- Bonding diagram respecting bonding and package constraints shall be generated
- ESD protection circuits shall be generated
- Clock distribution, including clock tree and buffers shall be generated
- Any other global networks that need P&R decisions shall be generated
- Final set of constraints and options for the layout generation shall be selected
- P&R shall be performed applying all layout constraints
- Final resources utilization shall be determined
  - E.g., die size, number of logic elements, and number of I/Os
- Describe any Design-For-Manufacturability strategies applied during layout generation
- Final ASIC post-layout netlist shall be generated applying manufacturer constraints and design rules and the new timing data extracted from the layout
  - E.g., pre-layout netlist can be optimized by local re-synthesis or physical or topography synthesis in order to obtain the final post-layout netlist
- Final FPGA P&R database files needed for FPGA layout verification shall be generated
  - E.g., timing files such as SDF used for netlist timing simulation or static timing analysis, pin out assignment reports or power consumption reports.
- Input files needed for generation of ASIC masks or for FPGA programming shall be generated
  - E.g., GDSII files for ASICs or programming bit stream files for FPGAs

ECSS-E-ST-20-40 Phases, Reviews and Outputs

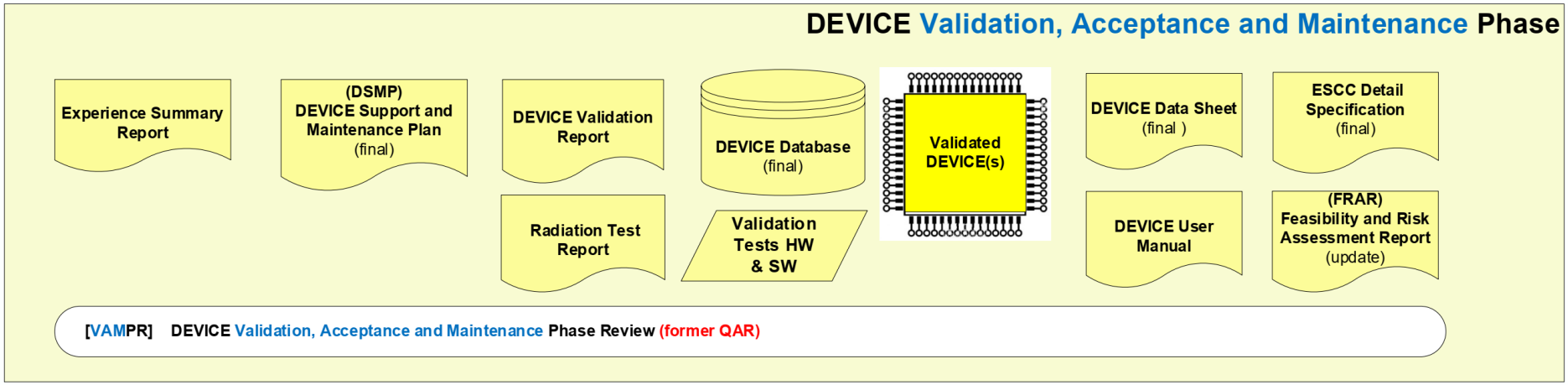


- **DEVICE Implementation Phase**:
  - Final ASIC DEVICE is manufactured, packaged and prototypes go through Production Tests in compliance with DEVICE Development Plan.
  - Final FPGA DEVICE is programmed, in compliance with DEVICE Development Plan
  - Phase concludes by delivery of tested DEVICES which undergo validation and customer acceptance in the DEVICE Validation, Acceptance and Maintenance Phase

Production and Test

- Committed number of DEVICEs using the technology choices specified in the DEVICE Development Plan shall be manufactured (ASIC) or programmed (FPGA)
- ASIC Production Tests shall be performed on the ASIC batch agreed between customer and supplier used for the validation tests during the DEVICE Validation, Acceptance and Maintenance Phase in compliance with DEVICE Validation Plan
- FPGA Programming Tests shall be performed on the same devices used for the validation tests during the DEVICE Validation, Acceptance and Maintenance Phase in compliance with DEVICE Validation Plan
- Generate the FPGA Programming Test Report including the following:
  - FPGA programming steps indicating compliance to FPGA tech. provider's "FPGA programming guidelines".
  - Input and output files, specifying format, identifier, version of netlist files, checksum and bit stream files used and generated during programming
  - HW and SW equipment used
  - The exact FPGA device part used, including serial number and manufacturing date

ECSS-E-ST-20-40 Phases, Reviews and Outputs



- **DEVICE Validation, Acceptance and Maintenance Phase**:
  - Manufactured (ASICs) or programmed (FPGA) parts already went through Production Tests (ASICs) or Programming Tests (FPGAs) undergo validation tests, as defined in the DEVICE Validation Plan
    - Radiation tests also if agreed with customer
  - Sometimes validation tests help to uncover problems or defects in DEVICE technology provided by the ASIC manufacturer or the DEVICE technology provider
  - Sometimes validation tests find design problems that were unfortunately not detected by verification due to tools or design kits limitations or not exhaustive verification coverage
  - With the data measured in all these tests, the existing versions of the DEVICE user and procurement documents, as agreed with the customer, are corrected and completed by the supplier
  - DEVICE Validation, Acceptance and Maintenance Phase Review, once declared successful, constitutes the acceptance by the customer of the outputs contractually agreed as deliverables
    - In some cases, contractually agreed deliverables can include some of the expected output hardware such as validation tests boards, and SW used for validation tests

Device Validation

- DEVICE validation shall be performed in compliance with the DEVICE Validation Plan
- Design and build the validation test set-up representative of the intended system application environment as defined in the DEVICE Validation Plan
- Use the validation test set-up to perform validation tests that cover all requirements in compliance with DEVICE Validation Plan
  - Requirements validated include functional, electrical, environmental, test modes and stress conditions.
- If agreed with customer and planned in the DEVICE Validation Plan, supplier shall perform ESCC evaluation or qualification tests
  - E.g. as defined in ESCC 9000 specifications: burn-in, V/T stress tests or any screening tests
- If agreed with customer and according to DEVICE Radiation Test Plan, supplier shall perform radiation tests and document the results in the Radiation Test Report

Experience Summary Report (ESR)

- Summary of main DEVICE development objectives and constraints
- Assessment of:
  - actual DEVICE development with respect to the original DEVICE Development Plan
  - controls, schedule, design iterations and communications
  - EDA tools adequacy, performance and major problems encountered
  - ASIC manufacturer or DEVICE technology provider support
- Summary of major problem areas found and solutions implemented during development
- If existing IP Cores were used, summary of lessons learned in terms of IP Core product quality and suitability
- Lessons learned and recommendations of interest for the customer and future suppliers of similar DEVICE developments

Summary of expected outputs of engineering flow

Development phase	Documentation	DEVICE models and SW	Hardware
DEVICE Definition Phase	DEVICE Requirements Specification (DRS) Feasibility and Risk Assessment Report (FRAR) DEVICE Development Plan (DDP) DEVICE Verification Plan (preliminary) (DVeP) DEVICE Validation Plan (preliminary) (DVaP) DEVICE Support and Maintenance Plan (preliminary) (DSMP)		
DEVICE Architecture Definition Phase	Architecture Definition Report DEVICE Verification Plan (update) (DVeP) DEVICE Validation Plan (update) (DVaP)		
DEVICE Design and Verification Phase	DEVICE Design Report Design Verification Report DEVICE Data Sheet (preliminary) DEVICE Verification Plan (final) (DVeP)	DEVICE Database containing: Simulation models (e.g. RTL) Verification results	
DEVICE Detailed Design Phase	Netlist Generation Report Netlist Verification Report DEVICE Data Sheet (update)	Updated DEVICE database containing: Pre-layout netlist Constraints for technology mapping and layout Preliminary test vectors for production	
DEVICE Layout Phase	Layout Generation Report Layout Verification Report DEVICE Validation Plan (final) (DVaP) Radiation Test Plan DEVICE Data Sheet (update) ESCC Detail Specification (preliminary)	Updated DEVICE database containing: Post-layout netlist Corresponding parasitic information ASIC files for manufacturer FPGA programming files Final Test Vectors	
DEVICE Implementation Phase	ASIC Production Tests Report FPGA Programming Test Report	Updated DEVICE database containing: Manufacturing or programming log and test files	Tested DEVICES
DEVICE Validation, Acceptance and Maintenance Phase	DEVICE Validation report Radiation Test Report DEVICE Data Sheet (final) ESCC Detail Specification (final) DEVICE User Manual Experience Summary Report DEVICE Support and Maintenance Plan (final)	DEVICE Database (final) Validation Tests software	Validation Tests hardware Validated DEVICES