dscal
DIGITAL SYSTEMS & COMPUTER ARCHITECTURE LABORATORY

Εργαστήριο Space Data Systems

4ο Εργαστηριακό Μάθημα

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ΤΜΗΜΑ
ΠΛΗΡΟΦΟΡΙΚΗΣ & ΤΗΛΕΠΙΚΟΙΝΩΝΙΩΝ

4η Εργαστηριακή Άσκηση

Ανάλυση άσκησης

A

Μετράω 10000000 χτύπους

=

1 sec

Υπολογισμός επόμενης κατάστασης

Ενημέρωση Τρέχουσας Κατάστασης

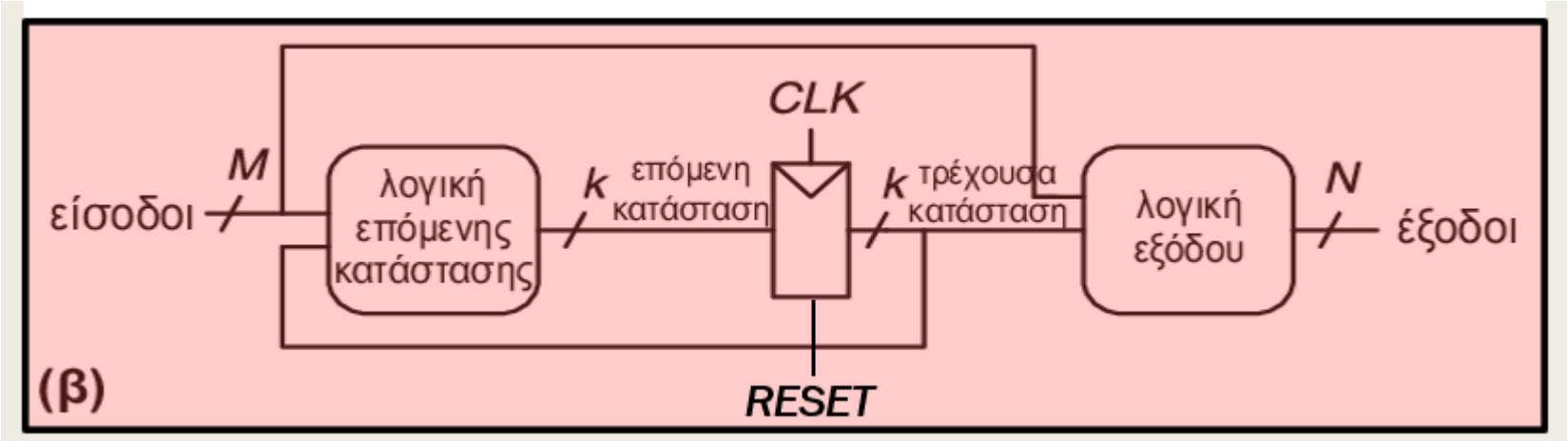
B

Μετράω δευτερόλεπτα

Υπολογισμός εξόδου

4η Εργαστηριακή Άσκηση

Ανάλυση άσκησης

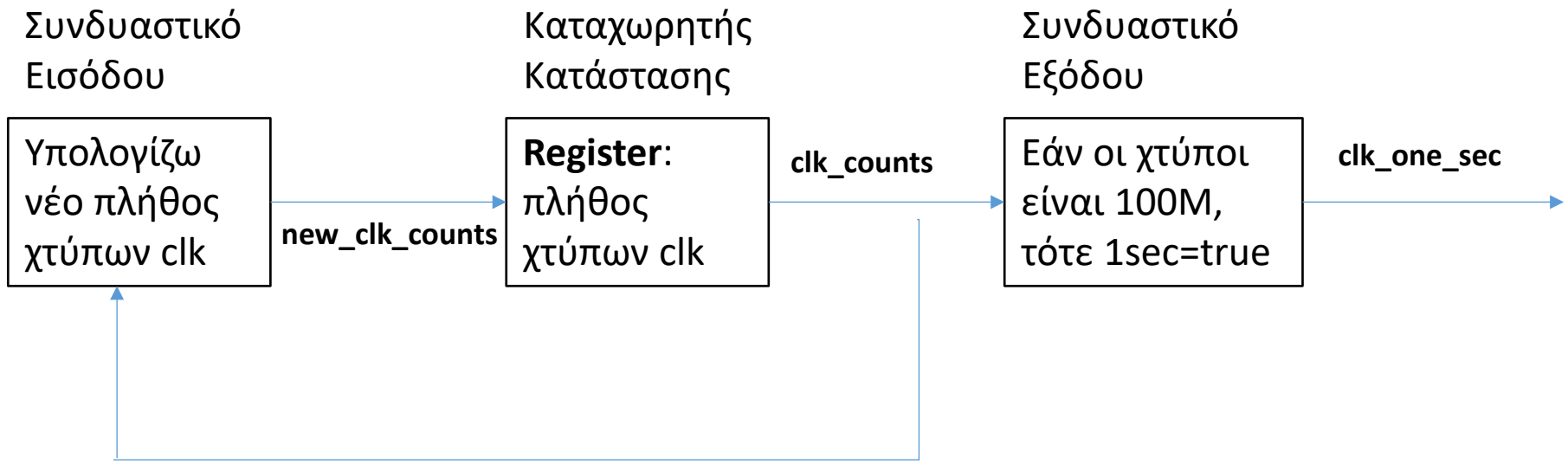


4η Εργαστηριακή Άσκηση

ΠΡΟΧΩΡΗΣΤΕ ΣΤΗΝ ΑΣΚΗΣΗ

4η Εργαστηριακή Άσκηση

Αρχιτεκτονική (1/6) – Νέο Ρολόι (Περίοδος = 1 sec)



4η Εργαστηριακή Άσκηση

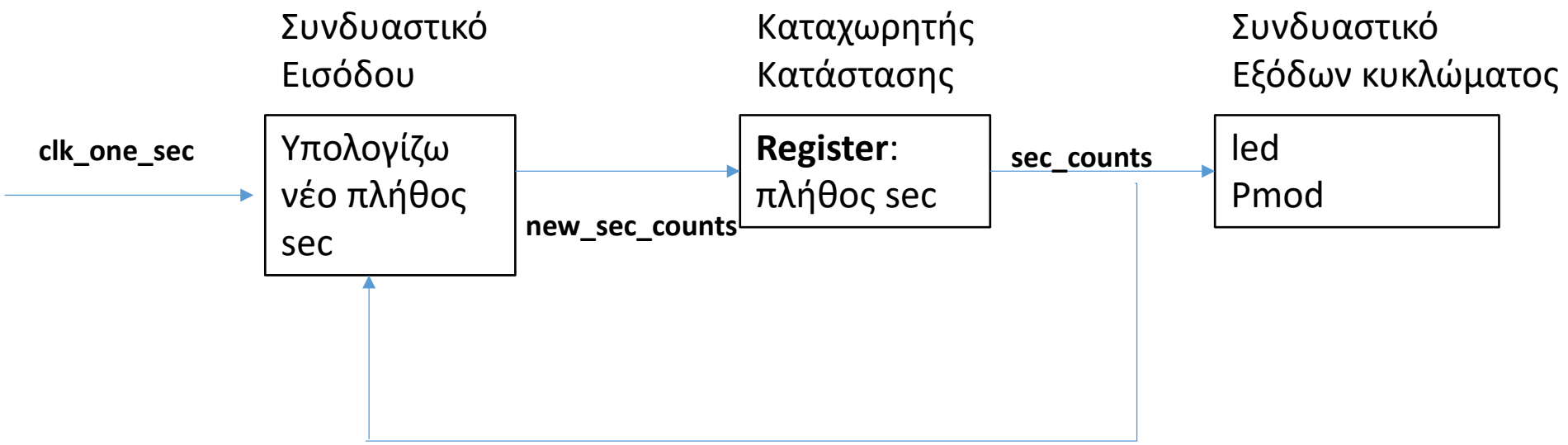
Αρχιτεκτονική (2/6) – Νέο Ρολόι (Περίοδος = 1 sec)

Αρχιτεκτονική →

```
new_clk_counts<=clk_counts+1 when clk_counts<100000000 else 0;

counts_100M : process (clk, reset) is

begin

        if reset = '1' then
                clk_counts<=0;
        elsif rising_edge(clk) then
                clk_counts<=new_clk_counts;
        end if; --reset

end process counts_100M;

clk_one_sec<='1' when clk_counts=100000000 else '0';
```

4η Εργαστηριακή Άσκηση

Αρχιτεκτονική (3/6) – Counter per second



4η Εργαστηριακή Άσκηση

Αρχιτεκτονική (4/6) –Counter per second

Αρχιτεκτονική →

```
process(clk_one_sec) is
begin

if (clk_one_sec='1') then
   if (direction='1' and sec_counts<99) then
      new_sec_counts<= sec_counts+1;
   elsif  (direction='0' and sec_counts>0) then
      new_sec_counts<= sec_counts-1;
   elsif  (direction='0' and sec_counts<=0) then
      new_sec_counts<= “1100011";
   elsif (direction='1' and sec_counts>=99) then
      new_sec_counts<="0000000";
   else
      new_sec_counts<="0000000";
   end if;
else
   new_sec_counts<=sec_counts;
end if;

end process;
```

```
count_seconds: process (clk, reset) is

begin

if (reset='1') then

   sec_counts<=(others=>'0');
elsif rising_edge(clk) then

   sec_counts<=new_sec_counts;

end if; --reset

end process count_seconds;
```

4η Εργαστηριακή Άσκηση

Αρχιτεκτονική (5/6) – Switch every 0.05 sec to each digit

Αρχιτεκτονική →

```
digit_process: process (clk, reset) is
variable clk_ticks : integer;
begin
if reset = '1' then
      clk_ticks :=0;
      digit_selection<='0';
      seven_segment<=(others=>'0');
elsif rising_edge(clk) then
      if clk_ticks = 500000 then
         clk_ticks := 0;
         digit_selection<=not digit_selection;
      else
         clk_ticks := clk_ticks + 1;
       end if; -- clk_ticks
end if; --reset
end process digit_process;
```

Άλλος τρόπος.
Χρήση variable

4η Εργαστηριακή Άσκηση

Αρχιτεκτονική (6/6) – Output signals

```
led_result<=std_logic_vector(sec_counts);
left_digit<=resize(sec_counts/10, left_digit'length);--Tens
right_digit<=resize(sec_counts mod 10, right_digit'length); --Units

left_digit_values: process (left_digit) begin
case left_digit is
   when X"0" => seven_segment_left   <="0111111";   -- 0
   when X"1" => seven_segment_left   <="0000110";   -- 1
   when X"2" => seven_segment_left   <="1011011";   -- 2
   when X"3" => seven_segment_left   <="1001111";   -- 3
   when X"4" => seven_segment_left   <="1100110";   -- 4
   when X"5" => seven_segment_left   <="1101101";   -- 5
   when X"6" => seven_segment_left   <="1111101";   -- 6
   when X"7" => seven_segment_left   <="0000111";   -- 7
   when X"8" => seven_segment_left   <="1111111";   -- 8
   when X"9" => seven_segment_left   <="1101111";   -- 9
   when others => seven_segment_left <="1000000";
end case;
end process left_digit_values;
```

```
right_digit_values: process (right_digit) begin
case right_digit is
   when X"0" => seven_segment_right   <="0111111";   -- 0
   when X"1" => seven_segment_right   <="0000110";   -- 1
   when X"2" => seven_segment_right   <="1011011";   -- 2
   when X"3" => seven_segment_right   <="1001111";   -- 3
   when X"4" => seven_segment_right   <="1100110";   -- 4
   when X"5" => seven_segment_right   <="1101101";   -- 5
   when X"6" => seven_segment_right   <="1111101";   -- 6
   when X"7" => seven_segment_right   <="0000111";   -- 7
   when X"8" => seven_segment_right   <="1111111";   -- 8
   when X"9" => seven_segment_right   <="1101111";   -- 9
   when others => seven_segment_right <="1000000";
end case;
end process right_digit_values;

digit_selection_out<=digit_selection;

seven_segment<=seven_segment_right when digit_selection='0' else
seven_segment_left when digit_selection='1' else (others=>'0');
```

4η Εργαστηριακή Άσκηση

Constraints (1/2) – CLK + Switches + Leds

Constraints →

```
# CLK - Zedboard 100MHz oscillator
set_property -dict { PACKAGE_PIN Y9 IOSTANDARD LVCMOS33 } [get_ports {clk}]

##############################
# On-board Slide Switches  #
##############################
set_property -dict { PACKAGE_PIN H17   IOSTANDARD LVCMOS33 } [get_ports { reset }];
set_property -dict { PACKAGE_PIN F22   IOSTANDARD LVCMOS33 } [get_ports { direction }];

##############################
# On-board LEDS  #
##############################
set_property -dict { PACKAGE_PIN T22   IOSTANDARD LVCMOS33 } [get_ports { led_result[0] }];
set_property -dict { PACKAGE_PIN T21   IOSTANDARD LVCMOS33 } [get_ports { led_result[1] }];
set_property -dict { PACKAGE_PIN U22   IOSTANDARD LVCMOS33 } [get_ports { led_result[2] }];
set_property -dict { PACKAGE_PIN U21   IOSTANDARD LVCMOS33 } [get_ports { led_result[3] }];
set_property -dict { PACKAGE_PIN V22   IOSTANDARD LVCMOS33 } [get_ports { led_result[4] }];
set_property -dict { PACKAGE_PIN W22   IOSTANDARD LVCMOS33 } [get_ports { led_result[5] }];
set_property -dict { PACKAGE_PIN U19   IOSTANDARD LVCMOS33 } [get_ports { led_result[6] }];
```

4η Εργαστηριακή Άσκηση

Constraints (2/2) – Pmod + CLK

Constraints →

```
##############################
# PmodSSO                    #
##############################

set_property -dict { PACKAGE_PIN Y11   IOSTANDARD LVCMOS33 } [get_ports { seven_segment[0] }];
set_property -dict { PACKAGE_PIN AA11  IOSTANDARD LVCMOS33 } [get_ports { seven_segment[1] }];
set_property -dict { PACKAGE_PIN Y10   IOSTANDARD LVCMOS33 } [get_ports { seven_segment[2] }];
set_property -dict { PACKAGE_PIN AA9   IOSTANDARD LVCMOS33 } [get_ports { seven_segment[3] }];
set_property -dict { PACKAGE_PIN W12   IOSTANDARD LVCMOS33 } [get_ports { seven_segment[4] }];
set_property -dict { PACKAGE_PIN W11   IOSTANDARD LVCMOS33 } [get_ports { seven_segment[5] }];
set_property -dict { PACKAGE_PIN V10   IOSTANDARD LVCMOS33 } [get_ports { seven_segment[6] }];

set_property -dict { PACKAGE_PIN W8   IOSTANDARD LVCMOS33 } [get_ports { digit_selection_out }];

##############################################################
##ZedBoard Timing Constraints
##############################################################
# define clock and period
create_clock -period 10 -name CLK -waveform {0.000 5.000} [get_ports {clk}]
```

4η Εργαστηριακή Άσκηση

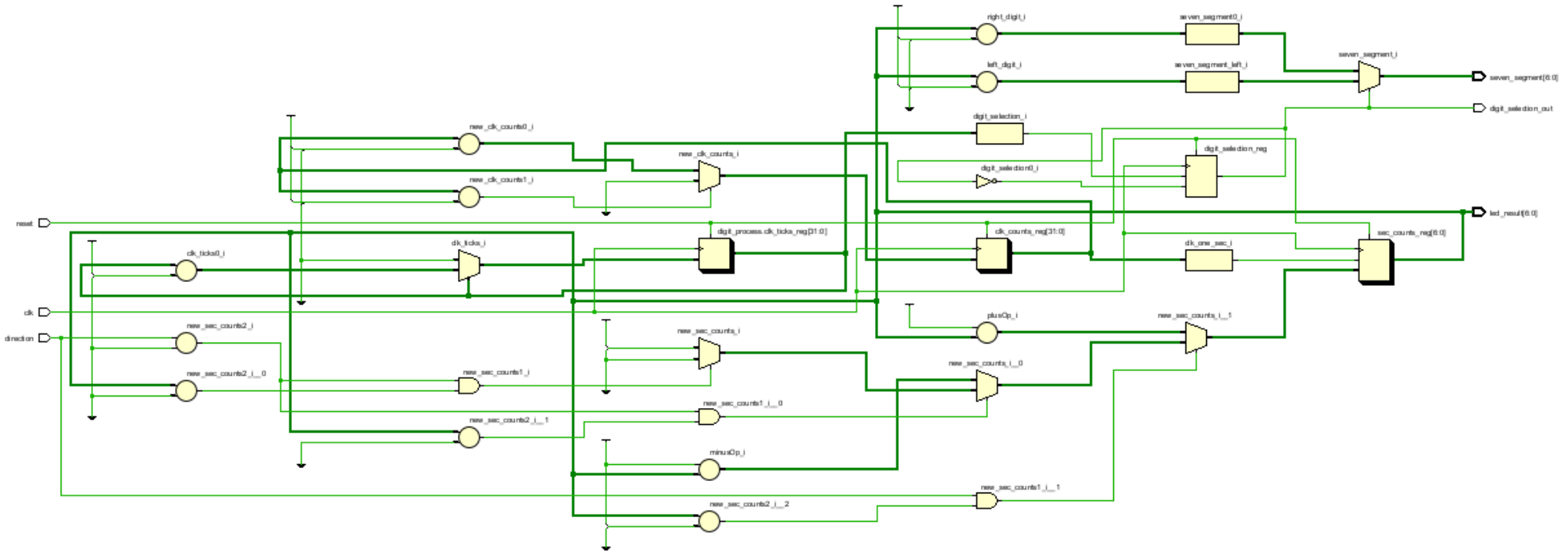
Pmod Manual

Manual Pmod

https://reference.digilentinc.com/reference/pmod/pmodssd/reference-manual

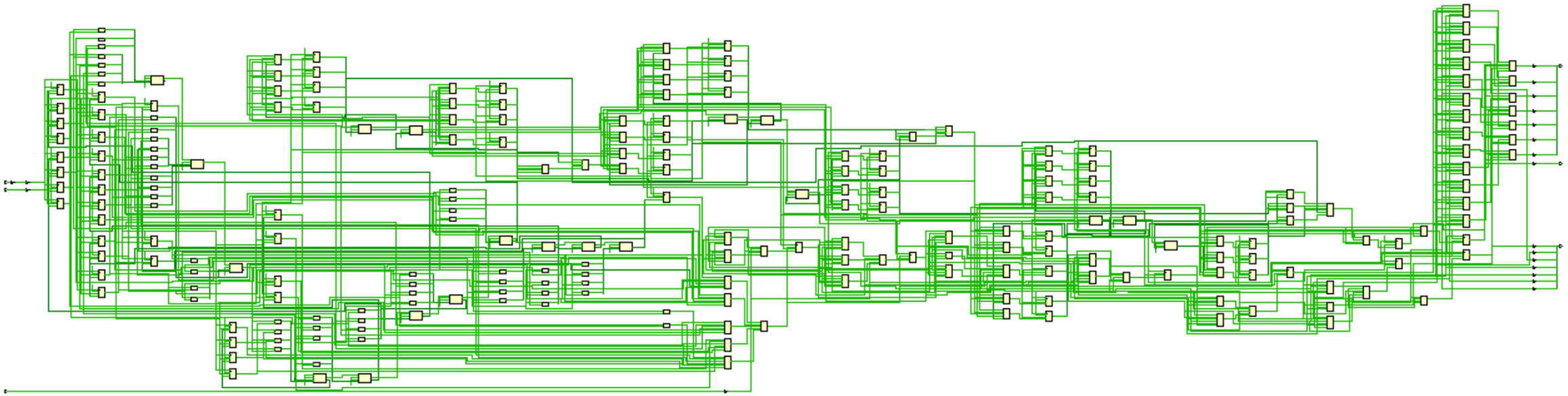
4η Εργαστηριακή Άσκηση

RTL Design



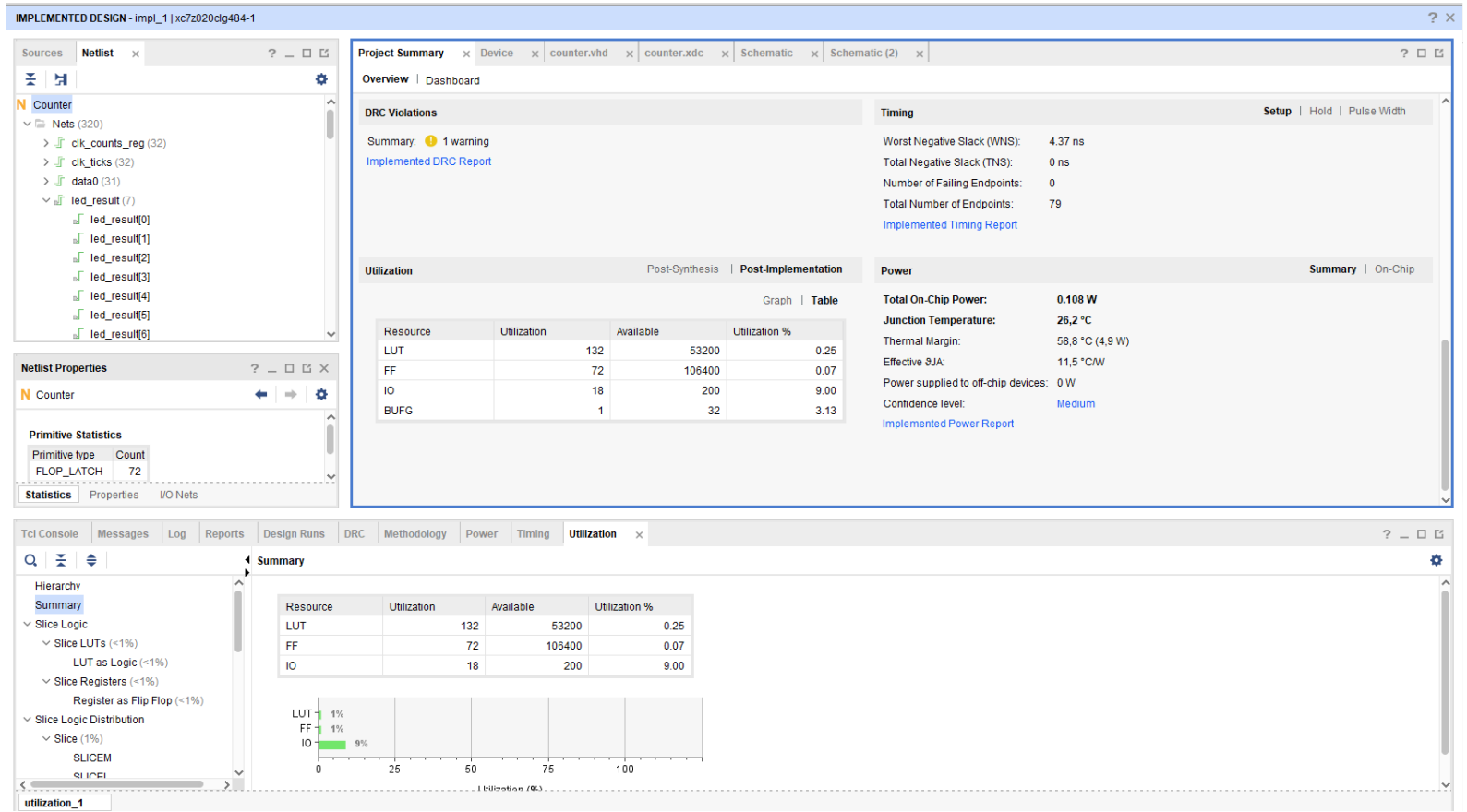
4η Εργαστηριακή Άσκηση

Synthesis/Implementation – Schematic



4η Εργαστηριακή Άσκηση

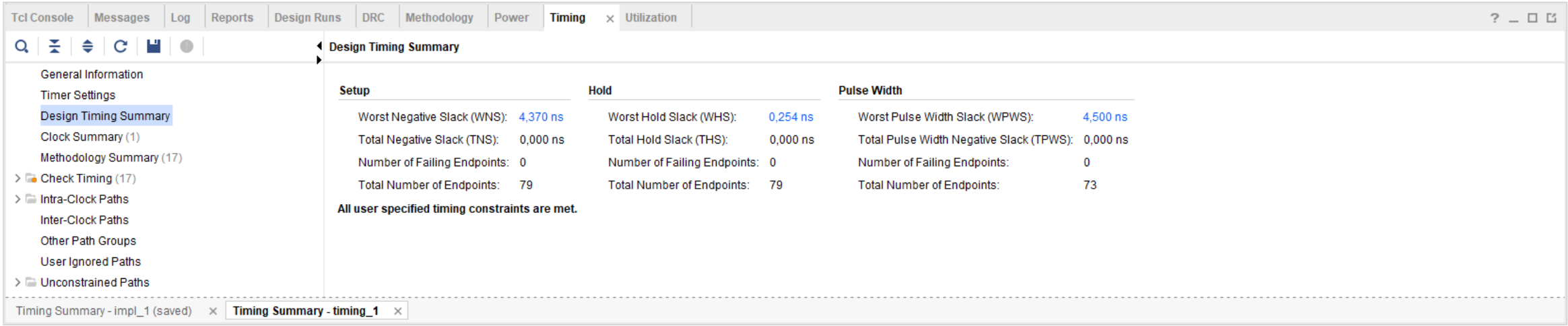
Implementation – Report Utilization



4η Εργαστηριακή Άσκηση

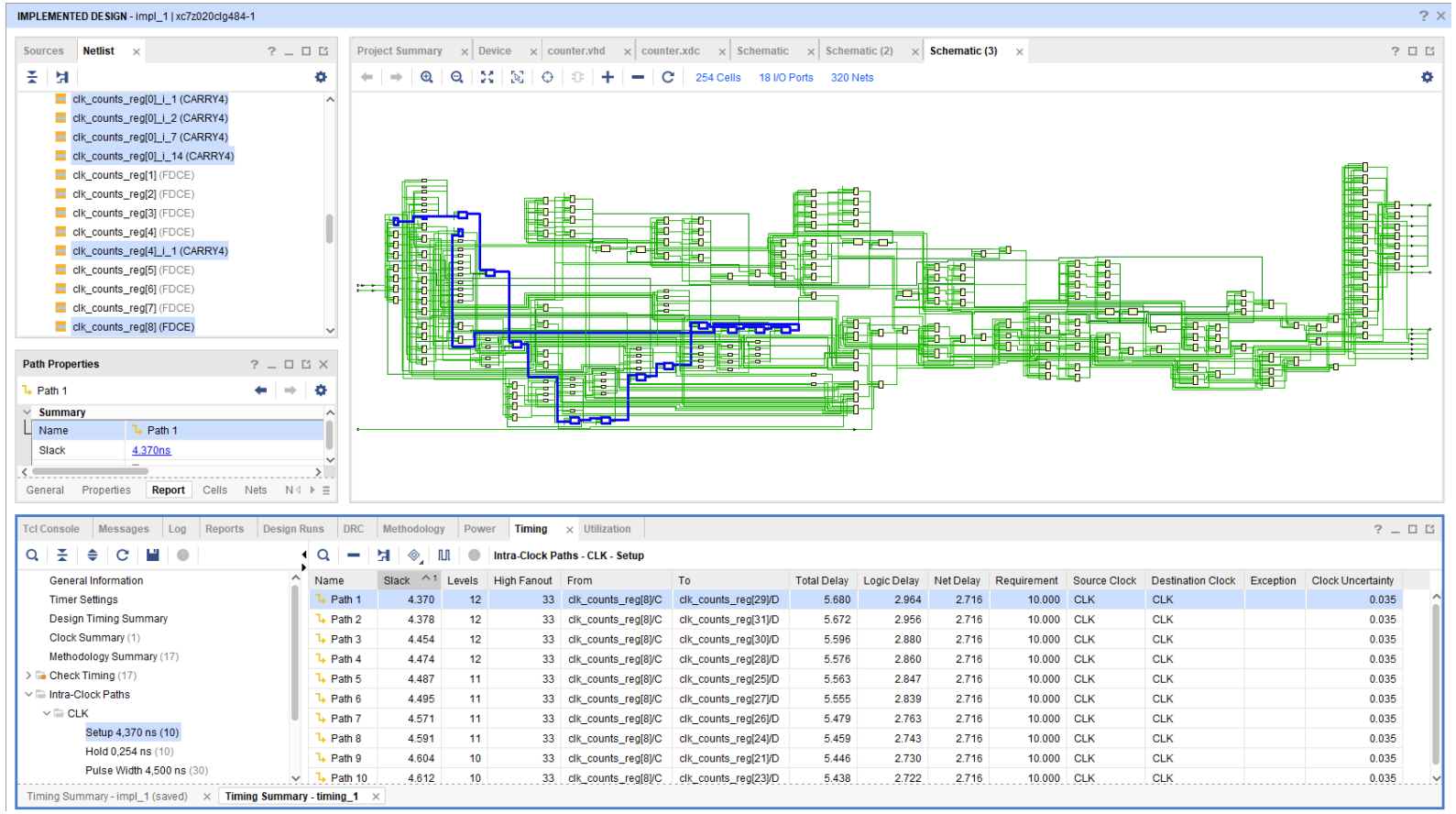
Implementation – Timing Reports (1/4)

Menu Reports->Timing-> Report Timing Summary
ή
Open Implemented Design->Report Timing Summary



4η Εργαστηριακή Άσκηση

Implementation – Timing Reports (2/4) - Setup

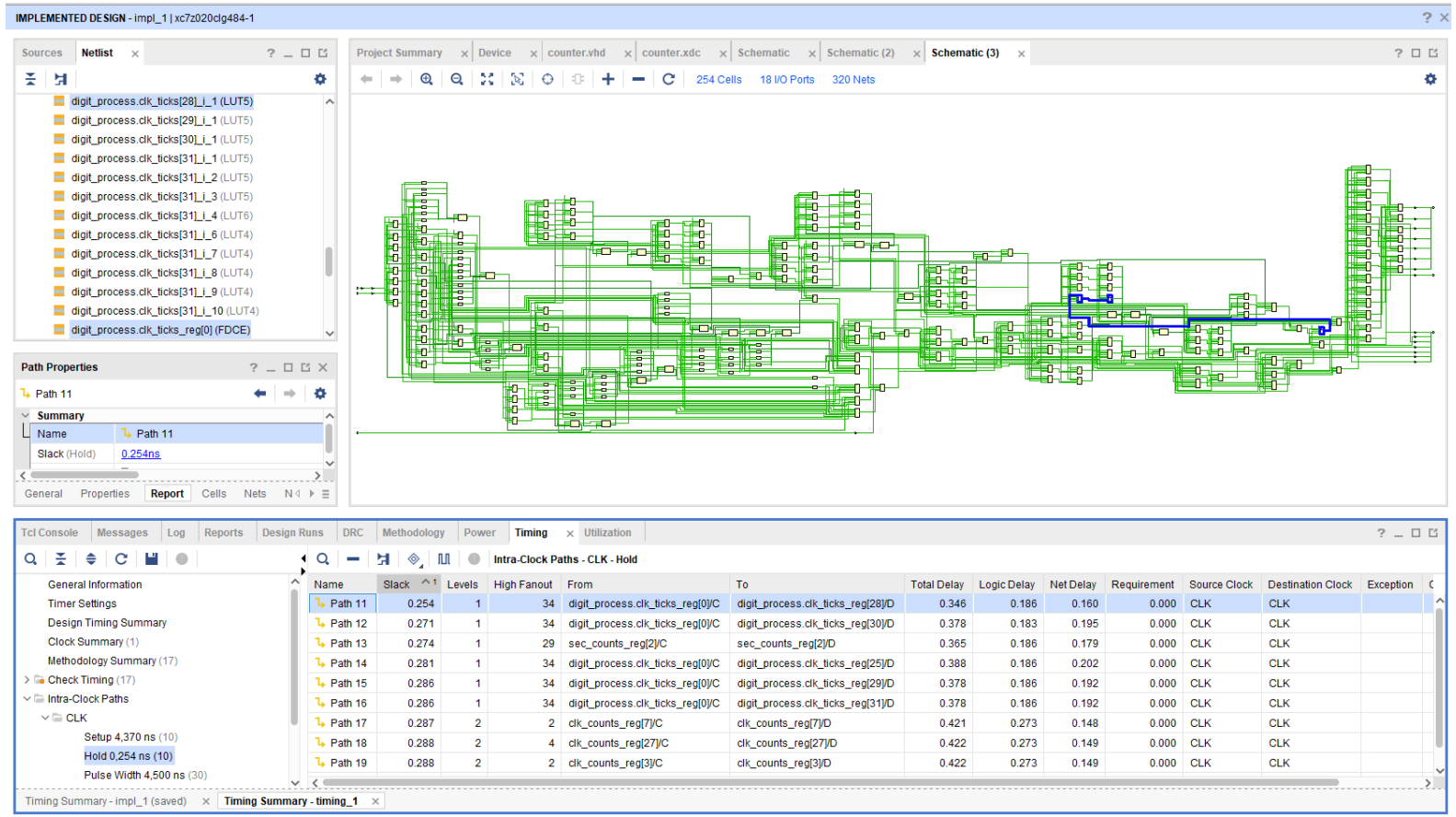


Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Exception	Clock Uncertainty
Path 1	4.370	12	33	clk_counts_reg[8]/C	clk_counts_reg[29]/D	5.680	2.964	2.716	10.000	CLK	CLK		0.035
Path 2	4.378	12	33	clk_counts_reg[8]/C	clk_counts_reg[31]/D	5.672	2.956	2.716	10.000	CLK	CLK		0.035
Path 3	4.454	12	33	clk_counts_reg[8]/C	clk_counts_reg[30]/D	5.596	2.880	2.716	10.000	CLK	CLK		0.035
Path 4	4.474	12	33	clk_counts_reg[8]/C	clk_counts_reg[28]/D	5.576	2.860	2.716	10.000	CLK	CLK		0.035
Path 5	4.487	11	33	clk_counts_reg[8]/C	clk_counts_reg[25]/D	5.563	2.847	2.716	10.000	CLK	CLK		0.035
Path 6	4.495	11	33	clk_counts_reg[8]/C	clk_counts_reg[27]/D	5.555	2.839	2.716	10.000	CLK	CLK		0.035
Path 7	4.571	11	33	clk_counts_reg[8]/C	clk_counts_reg[26]/D	5.479	2.763	2.716	10.000	CLK	CLK		0.035
Path 8	4.591	11	33	clk_counts_reg[8]/C	clk_counts_reg[24]/D	5.459	2.743	2.716	10.000	CLK	CLK		0.035
Path 9	4.604	10	33	clk_counts_reg[8]/C	clk_counts_reg[21]/D	5.446	2.730	2.716	10.000	CLK	CLK		0.035
Path 10	4.612	10	33	clk_counts_reg[8]/C	clk_counts_reg[23]/D	5.438	2.722	2.716	10.000	CLK	CLK		0.035

Setup Time:
Αναφέρεται στις αργές διαδρομές (καθυστέρηση διάδοσης)

4η Εργαστηριακή Άσκηση

Implementation – Timing Reports (3/4) - Hold



Hold Time:
Αναφέρεται στις γρήγορες διαδρομές (καθυστέρηση μόλυνσης)

4η Εργαστηριακή Άσκηση

Implementation – Timing Reports (4/4)

TCL Console>*report_timing_summary –datasheet*

(FULL REPORT)

Εμφανίζεται στη TCL console
(κοιτάξτε τα combinational delays)